GSTO

NAND Flash Memory

Serial Peripheral Interface (SPI)

GSS01GSAX1-W8NMI0

 Aug 12,2024

1 INTRODUCTION

1.1 General description

The GSS01GSAX1-W8NMI0 is a SPI (Serial Peripheral Interface) NAND Flash memory, with advanced write protection mechanisms.
The GSS01GSAX1-W8NMI0 supports the standard Serial Peripheral Interface (SPI), Dual/Quad I/O Operation.

FEATRUES

- **Voltage Supply**

–Vcc : 3.3V (2.7V~3.6V)

- **Organization**

–Density: (128M + 4M) Byte
–Page Size: (2048 + 64) Byte
–Block Size: (128K + 4K) Byte
–Device Size: 1Gb (1024 Blocks)

- **Serial Interface**

–Standard SPI: CLK, /CS, DI, DO, /WP, /Hold
–Dual SPI: CLK, /CS, DQ0, DQ1, /WP, /Hold
–Quad SPI: CLK, /CS, DQ0, DQ1, DQ2, DQ3
–Compatible SPI serial flash command

- **High Performance QSPI Nand Flash**

–108Mhz Standard/Dual/Quad SPI Clocks
–216/432Mhz equivalent Dual/Quad SPI
–2K-Byte cache for fast random read

- **ECC**

–8bit/512Byte BCH ECC(1)
–Internal data shaping support to increase data endurance (Randomize)

- **Program/Erase/Read Speed**

– Page Program time:450us typical

– Block Erase time: 3.5mstypical

– Page Read time:180us typical

- **Advanced Security feature**

–Software and Hardware Write-Protect
–ECC status bit indicate ECC result
–Bad block management and LUT (2) access
–Power Supply Lock-Down and OTP protection
–2KB Unique ID and 2KB Parameter pages
–Ten 2KB OTP pages (one-time programmable NAND Flash memory area)
–Write protect all/portion of memory via software

- **Wide Temperature Range**

–-40℃ to 85℃ operating range

- **Space Efficient Packaging**

–8-Pad WSON 8x6-mm

- **Reliability**

–10-years data retention (with 8bit/512Byte ECC)

Notes:

1) Internal ECC is always enabled even ECC-E is set to 0.
2) LUT stands for Look-Up Table.

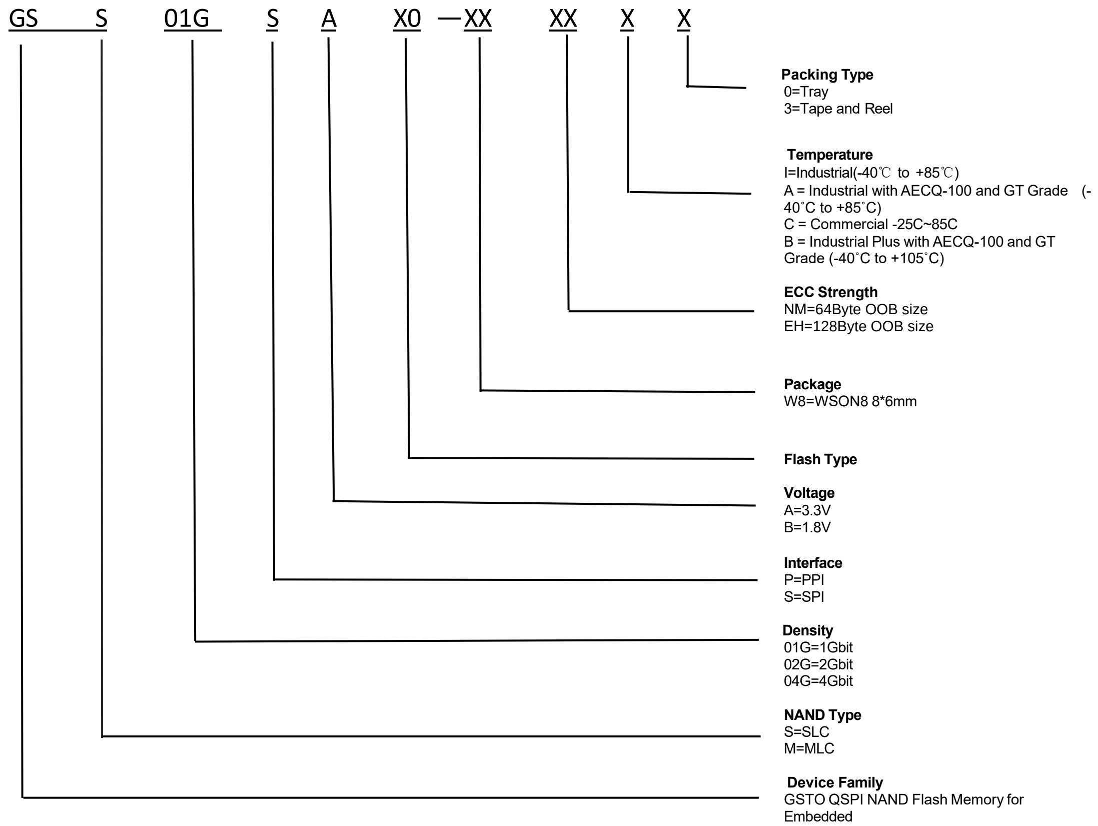
1.2 Product List

[Table 1-1] Product List

Part Number	MID	DID	Density	Organization	Package Type	Package Size(mm)	Vcc Range
GSS01GSAX1-W8NMI0	52h	CA13h	1 Gb	X1	WSON8	8x6	2.7V～3.6V

1.3 Part Numbering Rule

The ordering part number is formed by a valid combination of the following:

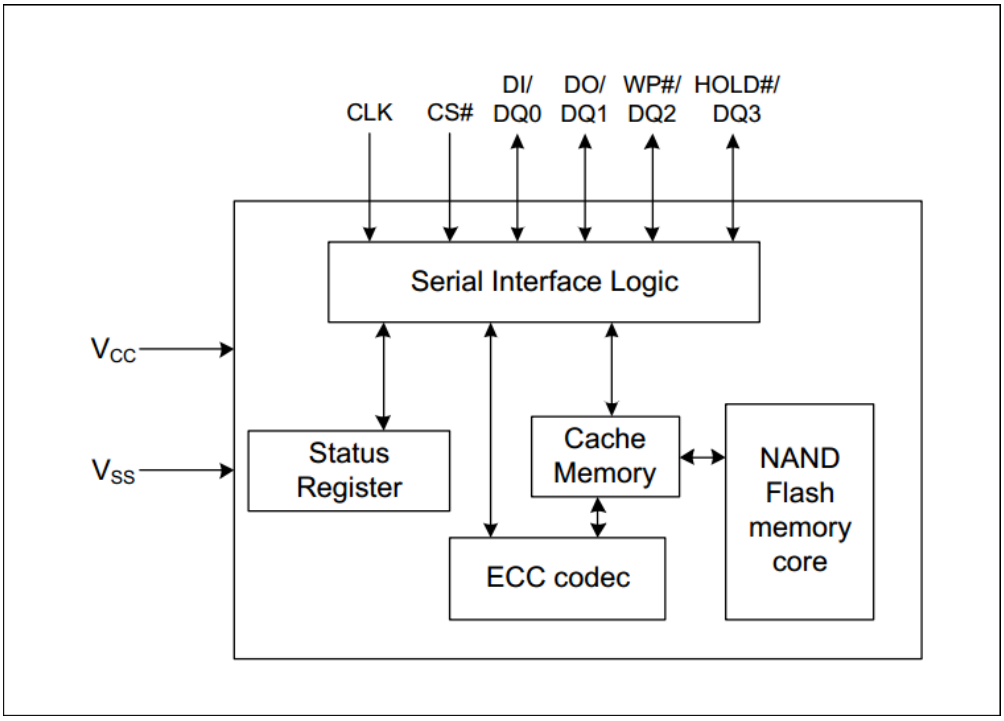


1.4 Revision History

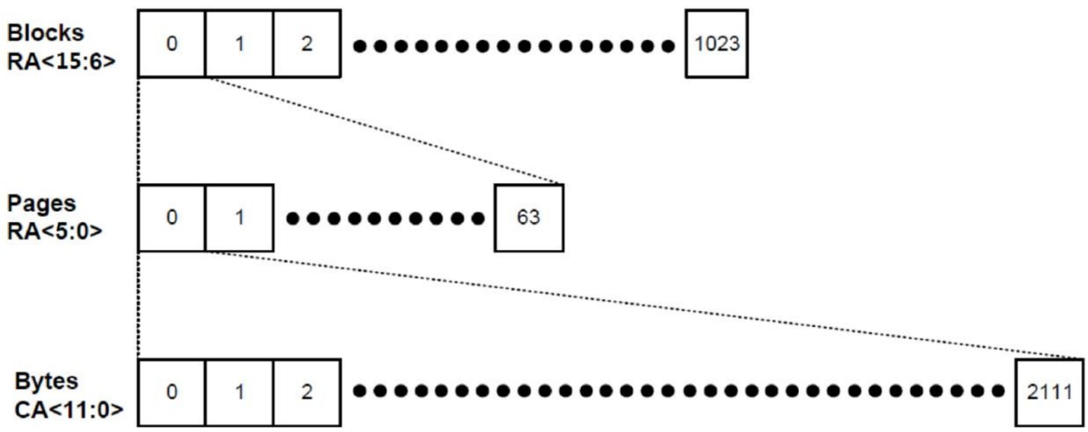
Version	Data	Page	Description
1.0	Jul 20	All	New create preliminary datasheet
1.1	Aug 12	34	Update ECC Status Bit Descriptions

2 Block Diagram

[Figure 2-1] SPI NAND Flash Memory Block Diagram



[Figure 2-2] Memory Map



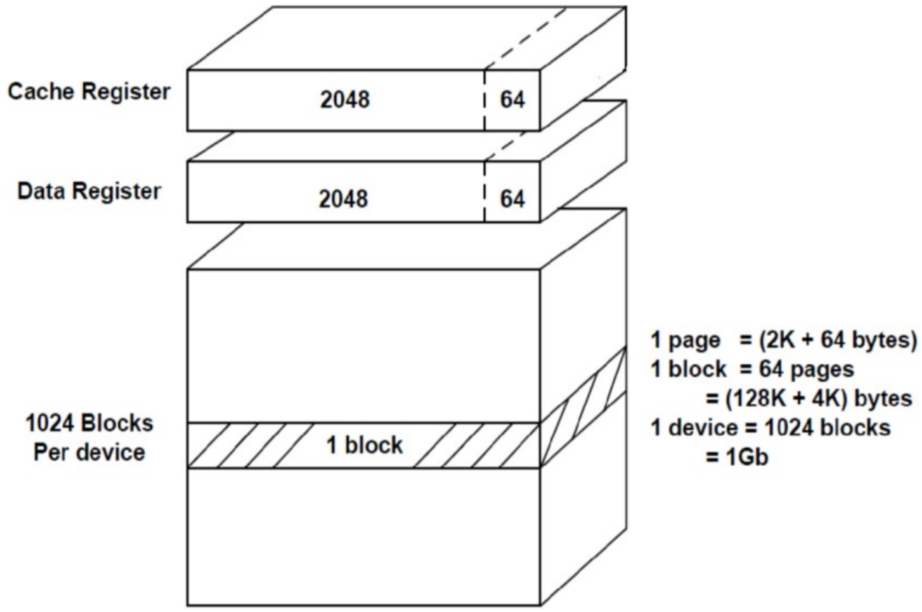
Note:

1) CA: Column Address. The 12-bit column address is capable of addressing from 0 to 4095 bytes; however,only bytes 0 through 2111 are valid. Bytes 2112 through 4095 of each page are “out of bounds”, do not exists in the device, and cannot be addressed.
2) RA: Row Address. RA<5:0> selects a page inside a block, and RA<15:6> selects a block.

[Table 2-3] Array Organization

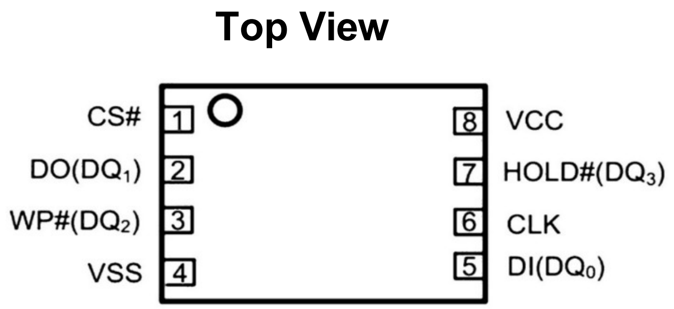
Each Device has	Each block has	Each page has	Unit
128M+4M	128K + 4K	2K+64	Bytes
1024 x 64	64	--	Pages
1024	--	--	Blocks

[Figure 2-4] Array Organization 1 Gb



3 Packaging Type and Pin Configurations

[Figure 3-1] Pad Assignments, WSON8 (8x6mm)



3.1 Pin Description

[Table 3-1] SPI Pin Description

Pin No.	Pin Name	I/O	Function
1	CS#	I	Chip Select Input
2	DO (DQ1)	I/O	Data Output (Data Input Output 1)(1)
3	WP# (DQ2)	I/O	Write Protect Input (Data Input Output 2)(2)
4	VSS		Ground
5	DI (DQ0)	I/O	Data Input (Data Input Output 0)(1)
6	CLK	I	Serial Clock Input
7	HOLD# (DQ3)	I/O	Hold Input (Data Input Output 3)(2)
8	VCC		Power Supply

Notes:

1. DQ0 and DQ1 are used for Dual SPI Interface.
2. DQ0 ~ DQ3 are used for Quad SPI Interface.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

[Table 4-1] Absolute Maximum

Rating	Value
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Voltage on I/O Pin with Respect to Ground	-0.5V to VCC+0.5V
VCC to Ground Potential	-0.5V to VCC+0.5V

Note:

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

4.2 Pin Capacitance

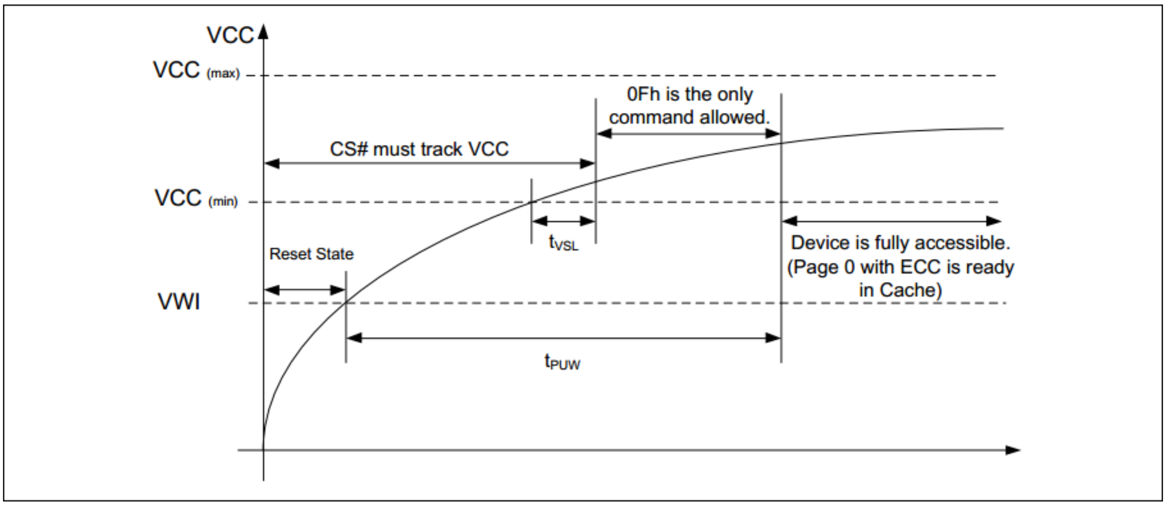
[Table 4-2] Pin Capacitance

Applicable over recommended operating range from: TA = +25°C, f = 1 MHz.

Symbol	Test Condition	Max	Units	Conditions
C_{IN}	Input Capacitance	6	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	8	pF	V_{OUT} = 0V

4.3 Power- On Timing

[Figure 4-1] Power- On Timing



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[Table 4-3] Power-On Timing and Write Inhibit Threshold

Parameter	Symbol	Min	Max	Unit
V_{CC} (min) to CS# Low	t_{VSL}	2		ms
Time Delay Before Write Instruction	t_{PUW}	12		ms
Write Inhibit Voltage	VWI		V_{CC}+0.5	V

4.4 DC Electrical Characteristics

[Table 4-4] DC Characteristics

Applicable over recommended operating range from: T_A= -40°C to +85°C, V_{CC}= 2.7V ~ 3.6V.

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
V_{CC}	Supply Voltage		2.7	3.3	3.6	V
I_{LI}	Input Leakage Current				±2	uA
I_{LO}	Output Leakage Current				±2	uA
I_{CC1}	Standby Current	V_{CC}=3.6V, CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}		50	100	μA
I_{CC2}	Operating Current (Read)	CLK=0.1V_{CC}/0.9V_{CC}		10	30	mA
I_{CC3}	Operating Current (Program)	CLK=0.1V_{CC}/0.9V_{CC}		10	30	mA
I_{CC4}	Operating Current (Erase)	CLK=0.1V_{CC}/0.9V_{CC}		15	30	mA
V_{IL}(1)	Input Low Voltage		-0.4		0.2V_{CC}	V
V_{IH}(1)	Input High Voltage		0.7V_{CC}		V_{CC}+0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -400μA	V_{CC}-0.2			V

Note:

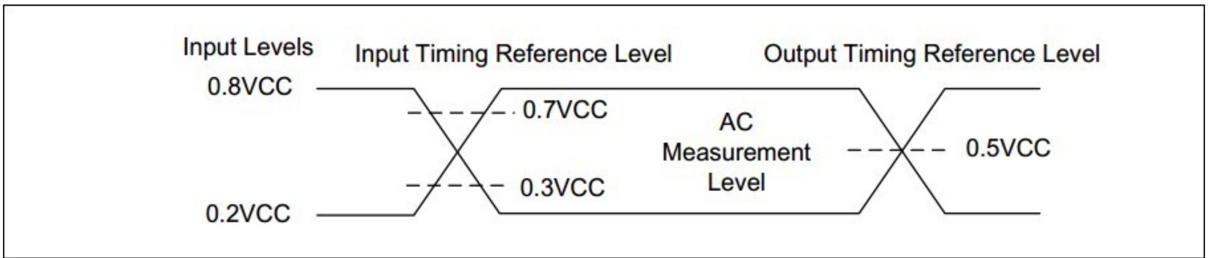
1. Tested on sample basis and specified through design and characterization data. TA = 25°C, VCC = 3.3V.

4.5 AC Measurement Conditions

[Table 4-5] AC Measurement Conditions

Symbol	Parameter	Min	Max	Typ.
C_L	Load Capacitance	–	30	pF
T_R, T_F	Input Rise and Fall Times	–	5	ns
V_{IN}	Input Pulse Voltages	0.2 VCC	0.8 VCC	V
IN	Input Timing Reference Voltages	0.3 VCC	0.7 VCC	V
OUT	Output Timing Reference Voltages	0.5VCC		V

[Figure 4-2] AC Measurement I/O Waveform



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4.6 AC Electrical Characteristics

[Table 4-6] AC Characteristics

Applicable over recommended operating range from: T_A= -40°C to +85°C, V_{CC}=2.7V ~ 3.6V。

Symbol	Parameter	Min	Typ.	Max	Unit
F_C	Serial Clock Frequency for: all command			104	MHz
t_{CH1}	Serial Clock High Time	5			ns
t_{CL1}	Serial Clock Low Time	5			ns
t_{CLCH}	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CHCL}	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
t_{SLCH}	CS# Active Setup Time relative to CLK	5			ns
t_{CHSH}	CS# Active Hold Time relative to CLK	5			ns
t_{SHCH}	CS# Not Active Setup Time relative to CLK	5			ns
t_{CHSL}	CS# Not Active Hold Time relative to CLK	5			ns
t_{SHSL}/t_{CS}	CS# High Time	20			ns
t_{SHQZ}	Output Disable Time			10	ns
t_{CLQX}	Output Hold Time	2			ns
t_{DVCH}	Data In Setup Time	2			ns
t_{CHDX}	Data In Hold Time	3			ns
t_{HLCH}	HOLD# Low Setup Time (relative to CLK)	5			ns
t_{HHCH}	HOLD# High Setup Time (relative to CLK)	5			ns
t_{CHHH}	HOLD# Low Hold Time (relative to CLK)	5			ns
t_{CHHL}	HOLD# High Hold Time (relative to CLK)	5			ns
t_{HLQZ}	HOLD# Low to High-Z Output			15	ns
t_{HHQX}	HOLD# High to Low-Z Output			15	ns
t_{CLQV}	Output Valid from CLK			8	ns
t_{WHSL}	WP# Setup Time before CS# Low	20			ns
t_{SHWL}	WP# Hold Time after CS# High	100			ns
tRST	CS# High to Next Command After Reset(FFh)			500	us
tRD	Page Read From Array		180	450	us
tPROG	Page Program		450	800	us
tERS	Block Erase		3.5	10	ms
NOP	Number of partial page program			1	time

Notes:

1. Clock high + Clock low must be less than or equal to 1/fC.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Tested on sample basis and specified through design and characterization data. TA = 25°C, VCC = 3.3V.

5 Device Operations

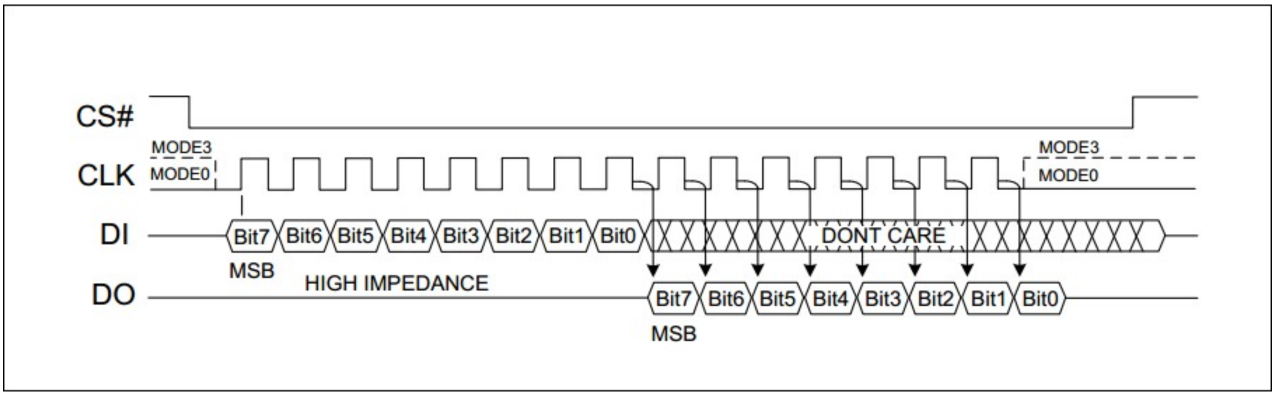
5.1 SPI Mode

5.1.1 Standard SPI

The GSS01GSAX1-W8NMI0 serial product is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (CS#), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Mode 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0, the CLK signal is normally low on the falling and rising edges of CS#. For Mode 3, the CLK signal is normally high on the falling and rising edges of CS#.

[Figure 5-1] SPI SDR Modes Supported



5.1.2 Dual SPI

The GSS01GSAX1-W8NMI0 serial product supports Dual SPI operation when using the x2 and dual IO instructions. These instructions allow data to be transferred to or from the device at two times the rate of ordinary Serial Flash devices. When using Dual SPI instructions, the DI and DO pins become bidirectional I/O pins: DQ0 and DQ1.

5.1.3 Quad SPI

The GSS01GSAX1-W8NMI0 serial product supports Quad SPI operation when using the x4 and Quad IO instructions.
These instructions allow data to be transferred to or from the device four times the rate of ordinary Serial Flash. When using Quad SPI instructions, the DI and DO pins become bidirectional DQ0 and DQ1 and the WP # and HOLD# pins become DQ2 and DQ3 respectively.

5.2 CS#

The SPI Chip Select (CS#) pin enables and disables device operation. When CS# is high, the device is deselected and the Serial Data Output (DO, or DQ0, DQ1, DQ2, DQ3) pins are at high impedance pulled by SPI HOST. When deselected, the devices power consumption will be at standby levels unless an internal erase, program, read, reset or individual block lock/unlock cycle is in progress. When CS# is brought low, the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, CS# must transition from high to low before a new instruction will be accepted.

5.3 CLK

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the CLK signal. Data output changes after the falling edge of CLK.

5.4 Serial Input (DI) / DQ0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial CLK clock signal. DI becomes DQ0 - an input and output during Dual and Quad commands for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

5.5 Serial Output (DO) / DQ1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial CLK clock signal. DO becomes DQ1 - an input and output during Dual and Quad commands for receiving addresses, and data to be programmed (values latched on rising edge of serial CLK clock signal) as well as shifting out data (on the falling edge of CLK).

5.6 Write Protect (WP#) / DQ2

When WP# is driven Low (VIL), during a SET FEATURES command and while the BRWD bit of the Status Register is set to a 1, it is not possible to write to the Status Registers. This prevents any alteration of the Block Protect (BP2, BP1, BP0), INV and CMP bits of the Status Register. As a consequence, all the data bytes in the memory area that are protected by the Block Protect (BP2, BP1, BP0), INV and CMP bits, are also hardware protected against data modification if WP# is Low during a SET FEATURES command. The WP# function is replaced by DQ2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

5.7 Hold (HOLD#) / DQ3

For Standard SPI and Dual SPI operations, the HOLD# signal allows the GSS01GSAX1-W8NMI0 serial product operation to be paused while it is actively selected (when CS# is low). The HOLD# function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the HOLD# function can save the state of the instruction and the data in the buffer also programming can resume where it left off once the bus is available again. To initiate a HOLD# condition, the device must be selected with CS# low. A HOLD# condition will activate on the falling edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will activate after the next falling edge of CLK. The HOLD# condition will terminate on the rising edge of the HOLD# signal if the CLK signal is already low. If the CLK is not already low the HOLD# condition will terminate after the next falling edge of CLK. During a HOLD# condition, the Serial Output (DO) is high impedance, and Serial Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (CS#) signal should be kept active (low) for the full duration of the HOLD# operation to avoid resetting the internal logic state of the device. The HOLD# function is not available when the Quad mode is enabled . The Hold function is replaced by DQ3 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the CLK signal) as well as shifting out data (on the falling edge of CLK).

6 COMMAND DEFINITIONS

6.1 Command Set Tables

Table 4 SPI NAND Command Set

Command	OP code	Byte2	Byte3	Byte4	Byte5	Byte6	Byte7	Byte8	Byte9
Reset	**FFh**								
Read ID	**9Fh**	Dummy	52h	CAh	13h				
Read Status Register	**0Fh**	SR Addr	S7-0	S7-0	S7-0	S7-0	S7-0	S7-0	S7-0
Write Status Register	**1Fh**	SR Addr	S7-0						
Write Enable	**06h**								
Write Disable	**04h**								
Block Erase	**D8h**	Dummy	PA15-8	PA7-0					
Program Data Load	**02h**	CA15-8	CA7-0	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Random Program Data Load	**84h**	CA15-8	CA7-0	Data-0	Data-1	Data-2	Data-3	Data-4	Data-5
Quad ProgramData Load	**32h**	CA15-8	CA7-0	Data-0/4	Data-1/4	Data-2/4	Data-3/4	Data-4/4	Data-5/4
Random Quad Program Data Load	**34h**	CA15-8	CA7-0	Data-0/4	Data-1/4	Data-2/4	Data-3/4	Data-4/4	Data-5/4
BB Management(Swap Blocks)	**A1h**	LBA	LBA	PBA	PBA				
Read BBM LUT	**A5h**	Dummy	LBA0	LBA0	PBA	PBA	LBA1	LBA1	LBA1
Program Execute	**10h**	PA23-16	PA15-8	PA7-0					
Page Data Read	**13h**	PA23-16	PA15-8	PA7-0					
Read	**03h**	CA15-8	CA7-0	Dummy	D7-0	D7-0	D7-0	D7-0	D7-0
Fast Read	**0Bh**	CA15-8	CA7-0	Dummy	D7-0	D7-0	D7-0	D7-0	D7-0
Fast Read Dual Output	**3Bh**	CA15-8	CA7-0	Dummy	D7-0 /2	D7-0 /2	D7-0 /2	D7-0 /2	D7-0 /2
Fast Read Quad Output	**6Bh**	CA15-8	CA7-0	Dummy	D7-0 /4	D7-0 /4	D7-0 /4	D7-0 /4	D7-0 /4
Fast Read Dual I/O	**BBh**	CA15-8/2	CA7-0 /2	Dummy/2	D7-0 /2	D7-0 /2	D7-0 /2	D7-0 /2	D7-0 /2
Fast Read Quad I/O	**EBh**	CA15-8/4	CA7-0 /4	Dummy/4	Dummy/4	D7-0 /4	D7-0 /4	D7-0 /4	D7-0 /4

Notes

1. Output designates data output from the device.
2. Column Address (CA) only requires CA[11:0], CA[15:12] are considered as dummy bits.
3. Page Address (PA) requires 24 bits. PA[23:6] is the address for 128KB blocks (total 1,024 blocks), PA[5:0] is the address for 2KB pages (total 64 pages for each block).
4. Logical and Physical Block Address (LBA & PBA) each consists of 16 bits. LBA[9:0] & PBA[9:0] are effective Block Addresses. LBA[15:14] is used for additional information.
5. Status Register Addresses:
   Status Register 1 / Protection Register: Addr = A0h
   Status Register 2 / Configuration Register: Addr = B0h
   Status Register 3 / Status Register: Addr = C0h
6. Dual SPI Address Input (CA15-8 / 2 and CA7-0 / 2) format:
   IO0 = x, x, CA10, CA8, CA6, CA4, CA2, CA0
   IO1 = x, x, CA11, CA9, CA7, CA5, CA3, CA1
7. Dual SPI Data Output (D7-0 / 2) format:
   IO0 = D6, D4, D2, D0, ...
   IO1 = D7, D5, D3, D1, ...
8. Quad SPI Address Input (CA15-8 / 4 and CA7-0 / 4) format:
   IO0 = x, CA8, CA4, CA0
   IO1 = x, CA9, CA5, CA1
   IO2 = x, CA10, CA6, CA2
   IO3 = x, CA11, CA7, CA3
9. Quad SPI Data Input/Output (*D7-0 / 4*) format:
   IO0 = D4, D0, ...
   IO1 = D5, D1, ...
   IO2 = D6, D2, ...
   IO3 = D7, D3, ...
10. All Quad Program/Read commands are disabled when WP-E bit is set to 1 in the Protection Register.

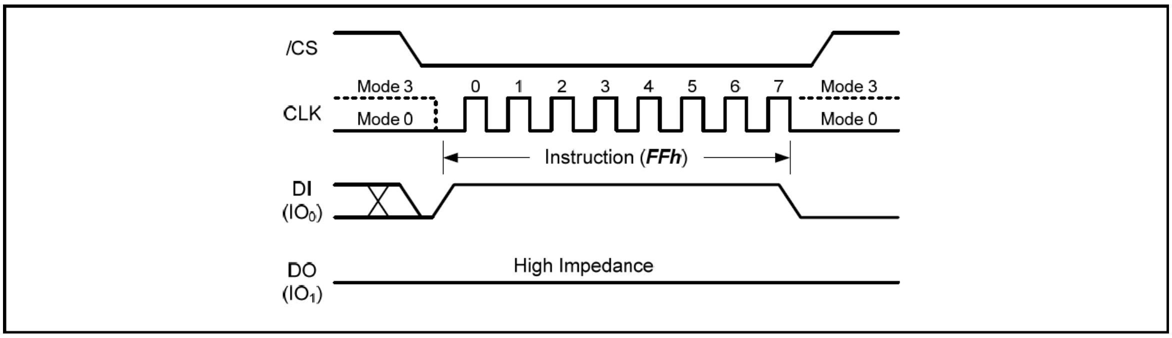
7 Initialization Operation

7.1 Reset Operation (FFh)

The GSS01GSAX1-W8NMI0 serial product provide a software Reset instruction instead of a dedicated RESET pin. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits. Once the Reset command is accepted by the device, the device will take approximately tRST to reset, depending on the current operation the device is performing, tRST can be 5us~500us. During this period, no command will be accepted.

Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit in Status Register before issuing the Reset command.

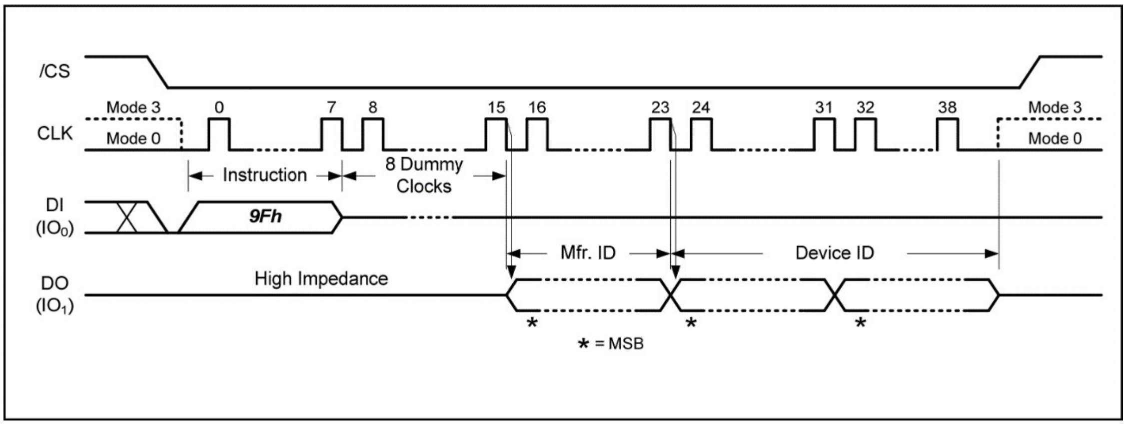
[Figure 7-1] RESET (FFh) Timing



7.2 Read JEDEC ID (9Fh)

The Read JEDEC ID command is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the CS# pin low and shifting the instruction code “9Fh” followed by 8 dummy clocks. The JEDEC assigned Manufacturer ID byte for GSTO (52h)and two Device ID bytes are then shifted out on the falling edge of CLK with most significant bit (MSB) first. For memory type and capacity values refer to Manufacturer and Device Identification table.

[Figure 7-2] READ JEDEC ID (9Fh) Timing

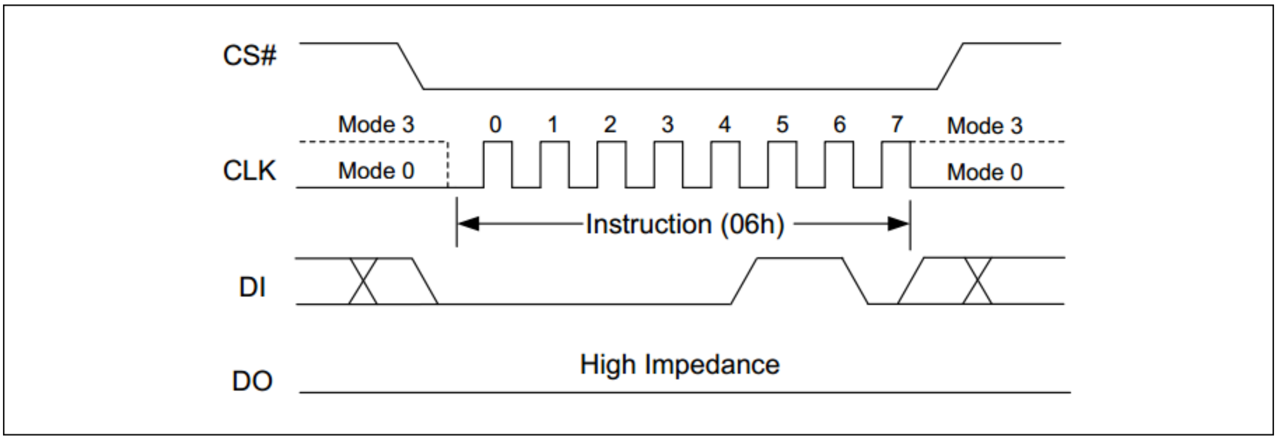


8 Write Operation

8.1 Write Enable (06h)

The Write Enable instruction sets the Write Enable Latch (WEL) bit in the Status Register to a 1.
The WEL bit must be set prior to every Page Program, Quad Page Program, Block Erase and Bad Block Management instruction. The Write Enable instruction is entered by driving CS# low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving CS# high.

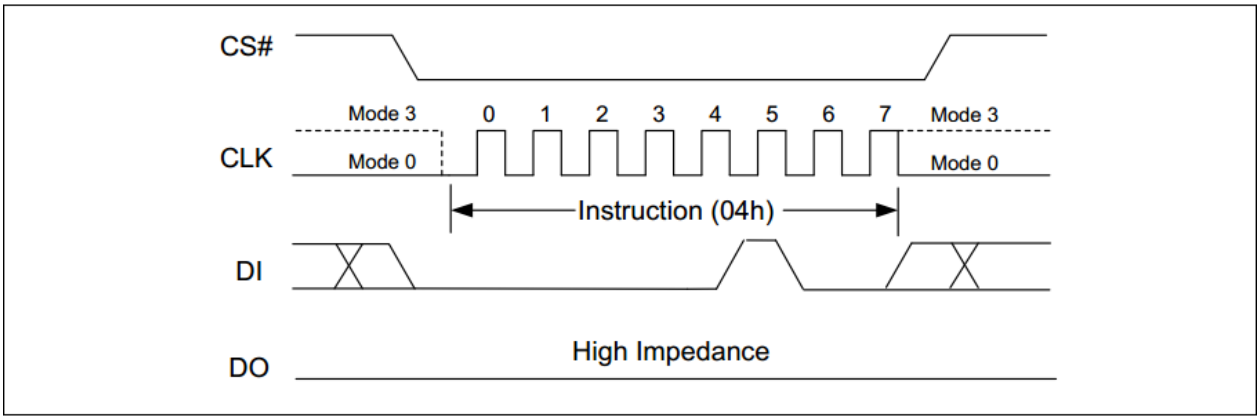
[Figure 8-1] Write Enable (06h) Timing



8.2 Write Disable (04h)

The Write Disable instruction resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving CS# low, shifting the instruction code “04h” into the DI pin and then driving CS# high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Page Program, Quad Page Program, Block Erase, Reset and Bad Block Management instructions.

[Figure 8-2] Write Disable (04h) Timing



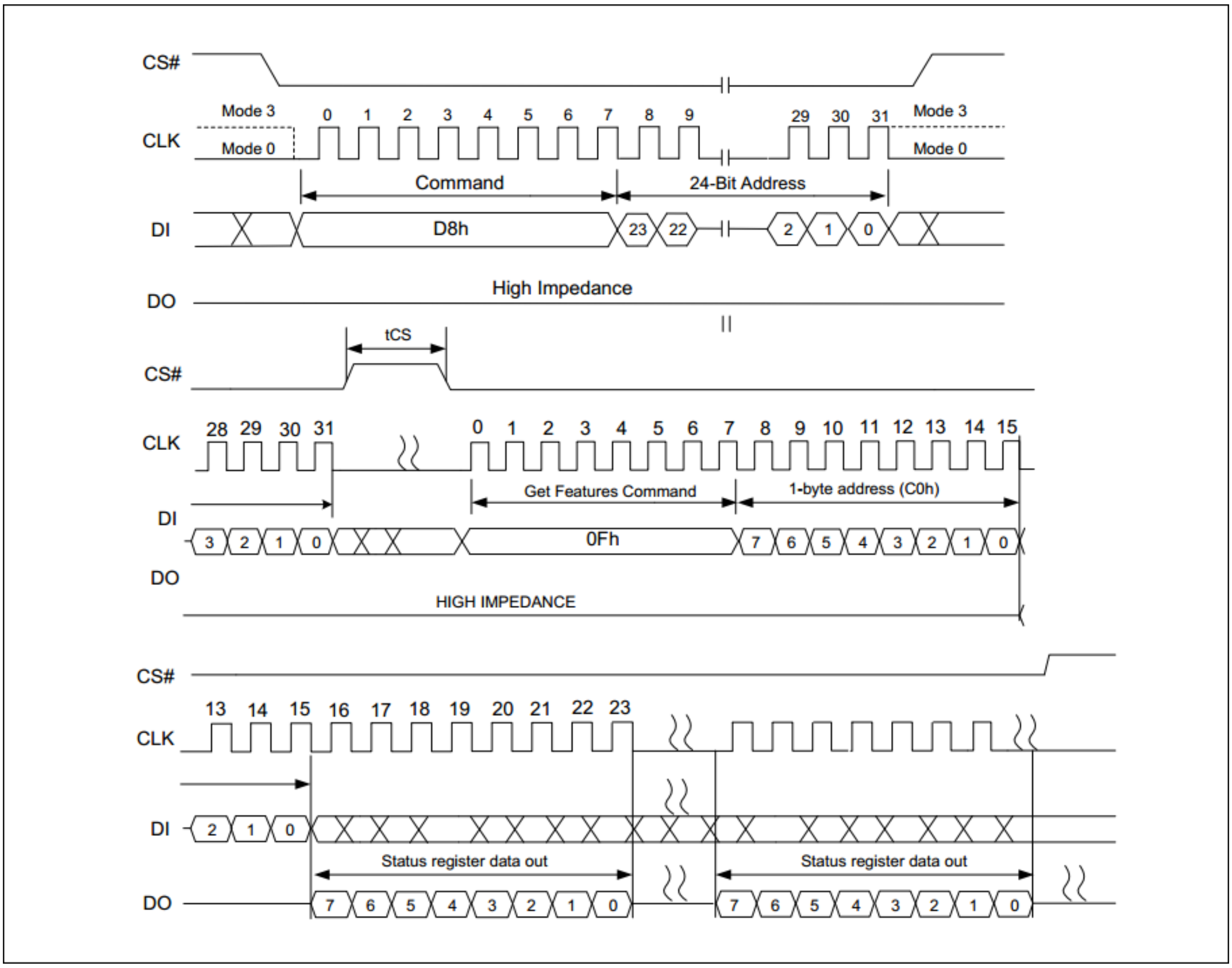
9 Erase Operation

9.1 128KB Block Erase (D8h)

The 128KB Block Erase instruction sets all memory within a specified block (64-Pages, 128K-Bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the CS# pin low and shifting the instruction code “D8h” followed by the 24-bit page address.

The CS# pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After CS# is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed block is protected by the Block Protect (TB, BP2, BP1, and BP0) bits.

[Figure 9-1] Block Erase (D8h) Timing



10 Program Operation

10.1 Load Program Data (02h) / Random Load Program Data (84h)

The Program operation allows from one byte to 2,112 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Program operation involves two steps:

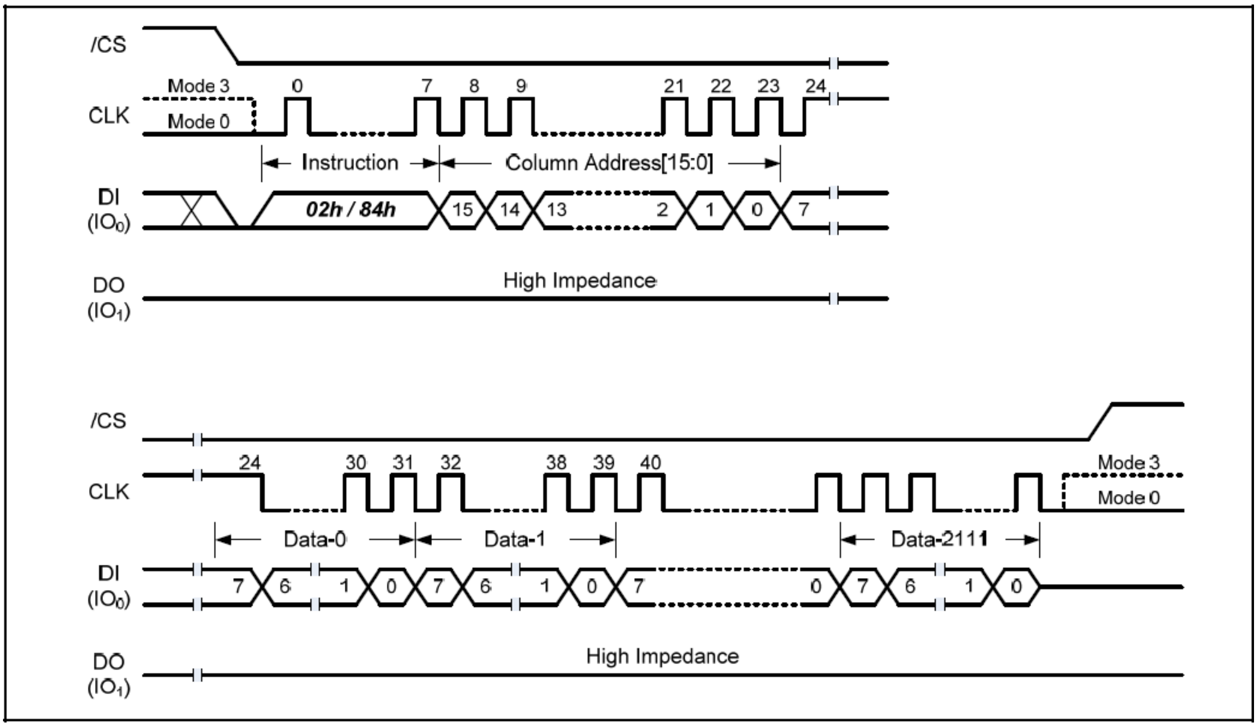
1) Load the program data into the Data Buffer.
2) Issue "Program Execute" command to transfer the data from Data Buffer to the specified memory page.

A Write Enable instruction must be executed before the device will accept the Load Program Data Instructions (Status Register bit WEL= 1). The "Load Program Data" or "Random Load Program Data" instruction is initiated by driving the CS# pin low then shifting the instruction code "02h" or "84h" followed by a 16-bit column address (only CA[11:0] is effective) and at least one byte of data into the DI pin. The CS# pin must be held low for the entire length of the instruction while data is being sent to the device. If the number of data bytes sent to the device exceeds the number of data bytes in the Data Buffer, the extra data will be ignored by the device.

Both "Load Program Data" and "Random Load Program Data" instructions share the same command sequence. The difference is that "Load Program Data" instruction will reset the unused the data bytes in the Data Buffer to FFh value, while "Random Load Program Data" instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

No matter internal ECC algorithm is enabled or disabled, all 2,112 bytes of data will be accepted. If the ECC-E bit is set to a 1, the values of ECC-0 and ECC-1 bit of C0 Register will indicate the ECC status.

[Figure 10-1] Load/Random Load Program Data (02h/84h) Timing



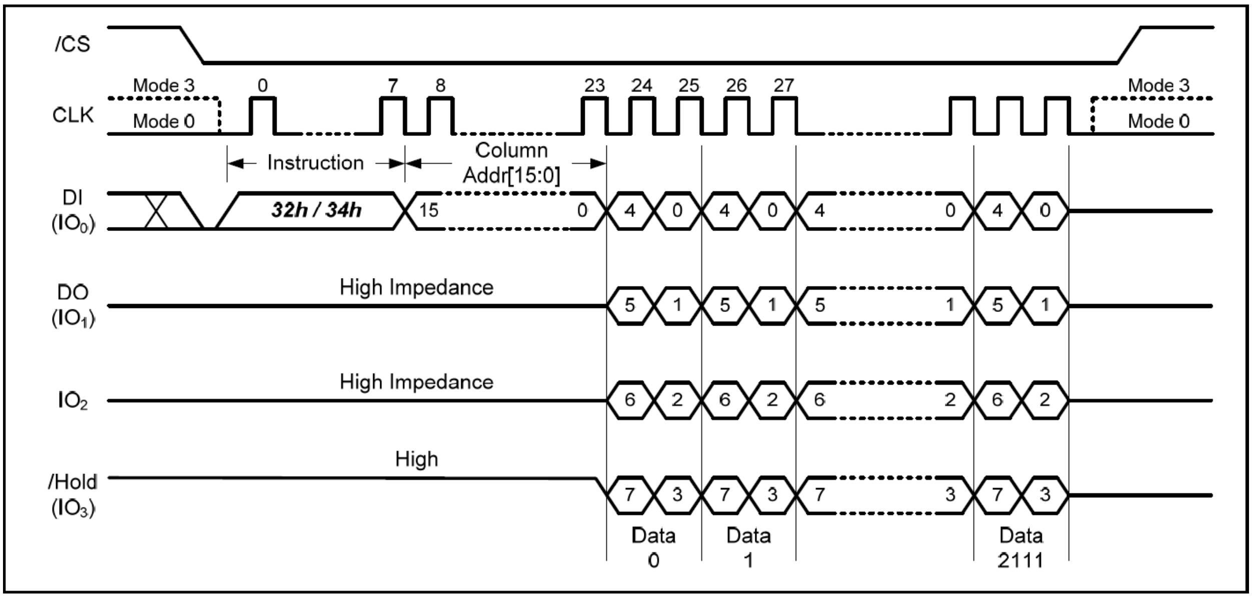
10.2 Quad Load Program Data (32h) /Quad Random Load Program Data (34h)

The “Quad Load Program Data” and “Quad Random Load Program Data” instructions are identical to the “Load Program Data” and “Random Load Program Data” in terms of operation sequence and functionality. The only difference is that “Quad Load” instructions will input the data bytes from all four IO pins instead of the single DI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the Data Buffer.

Both “Quad Load Program Data” and “Quad Random Load Program Data” instructions share the same command sequence. The difference is that “Quad Load Program Data” instruction will reset the unused the data bytes in the Data Buffer to FFh value, while “Quad Random Load Program Data” instruction will only update the data bytes that are specified by the command input sequence, the rest of the Data Buffer will remain unchanged.

When WP-E bit in the Status Register is set to a 1, all Quad SPI instructions are disabled.

[Figure 10-2] **Quad Load / Quad Random Load Program Data Timing**



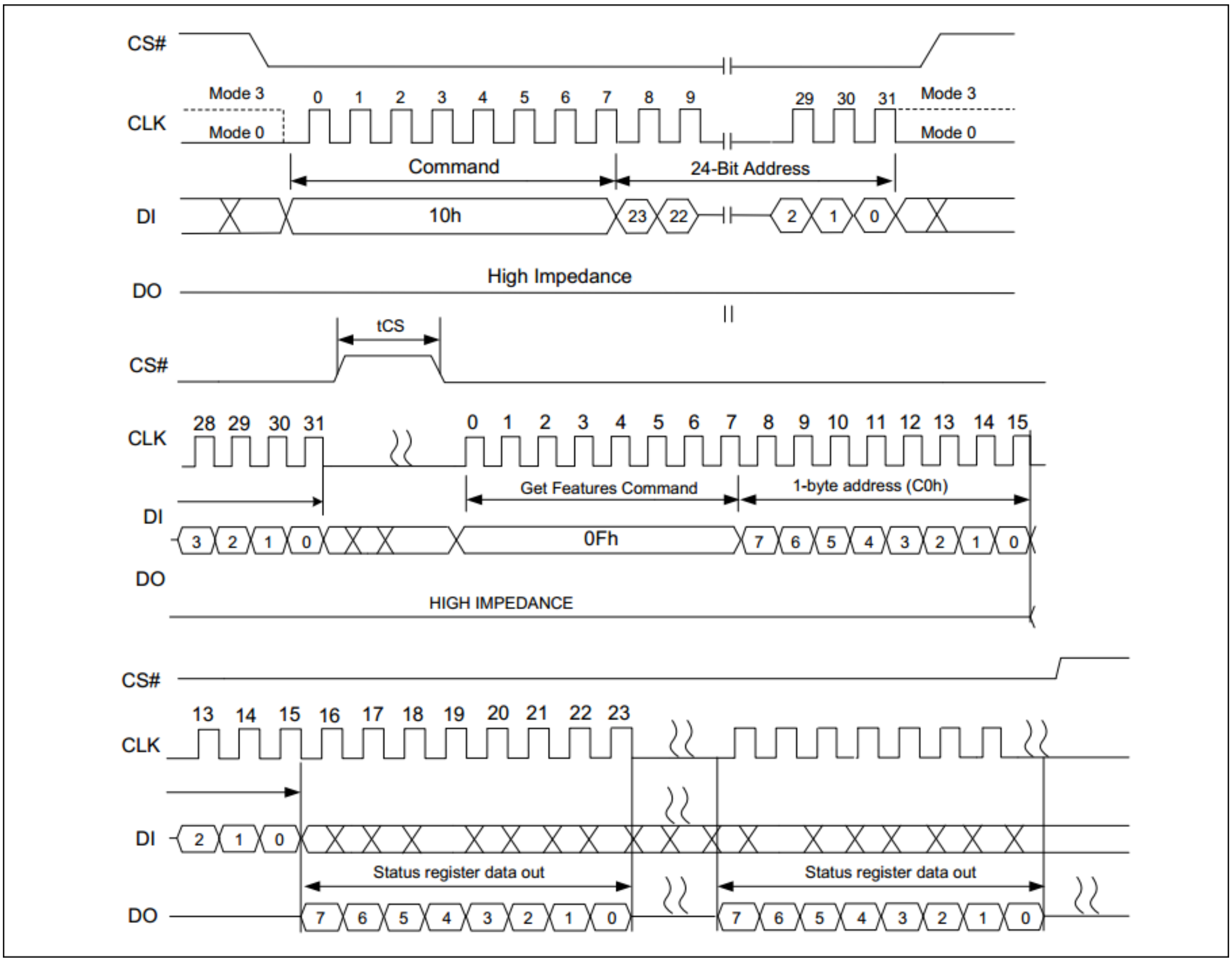
10.3 Program Execute (10h)

The Program Execute instruction is the second step of the Program operation. After the program data are loaded into the 2,112-Byte Data Buffer (or 2,048 bytes when ECC is enabled), the Program Execute instruction will program the Data Buffer content into the physical memory page that is specified in the instruction. The instruction is initiated by driving the CS# pin low then shifting the instruction code "10h" followed by 8-bit dummy clocks and the 16-bit Page Address into the DI pin as shown in Figure 17.

After CS# is driven high to complete the instruction cycle, the self-timed Program Execute instruction will commence for a time duration of tpp (See AC Characteristics). While the Program Execute cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Program Execute cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Program Execute cycle has finished, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Program Execute instruction will not be executed if the addressed page is protected by the Block Protect (TB, BP2, BP1, and BP0) bits. Only 4 partial page program times are allowed on every single page.

The pages within the block have to be programmed sequentially from the lower order page address to the higher order page address within the block. Programming pages out of sequence is prohibited.

[Figure 10-3] Program Execute (10h) Timing



11 Read Operation

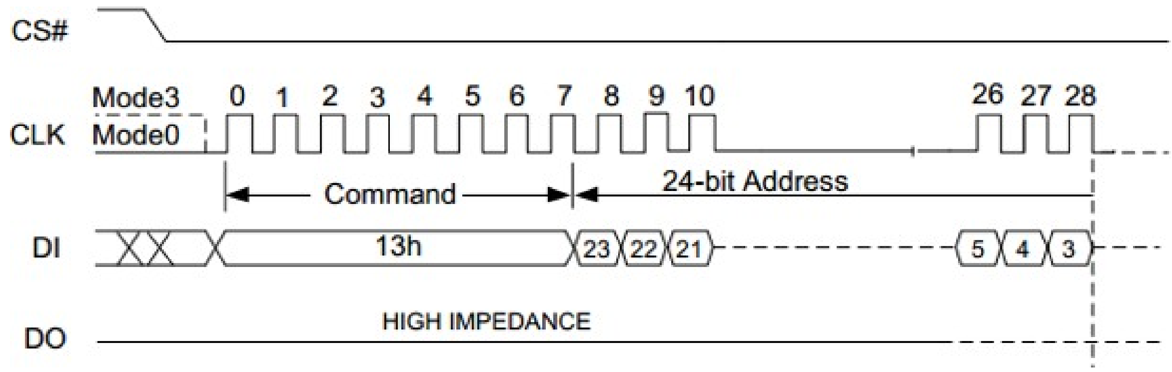
11.1 Page Read (13h)

The Page Data Read instruction will transfer the data of the specified memory page into the 2,112-Byte Data Buffer. The instruction is initiated by driving the CS# pin low then shifting the instruction code “13h” followed by 8-bit dummy clocks and the 16-bit Page Address into the DI pin as shown in Figure 18.

After CS# is driven high to complete the instruction cycle, the self-timed Read Page Data instruction will commence for a time duration of tRD (See AC Characteristics). While the Read Page Data cycle is in progress, the Read Status Register instruction may still be used for checking the status of the BUSY bit. The BUSY bit is a 1 during the Read Page Data cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.

After the 2,112 bytes of page data are loaded into the Data Buffer, several Read instructions can be issued to access the Data Buffer and read out the data.

[Figure 11-1] Page Read (13h) Timing

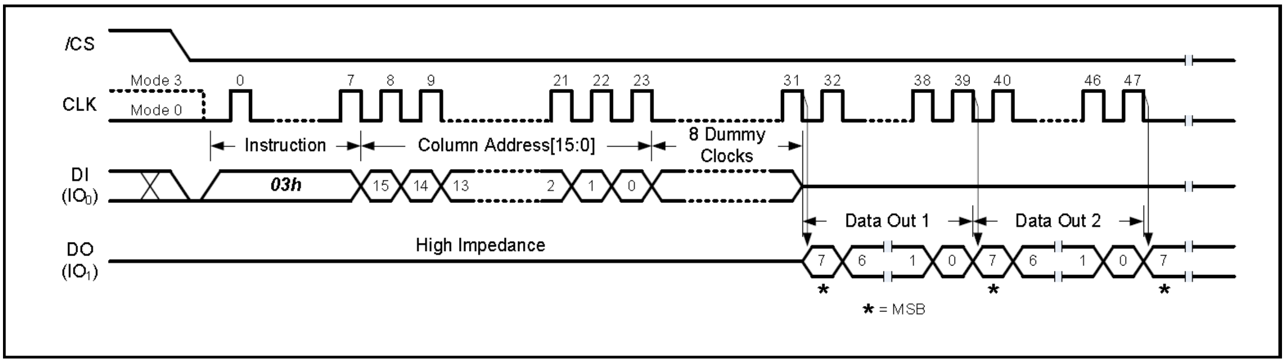


11.2 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Read Data instruction is initiated by driving the CS# pin low and then shifting the instruction code “03h” followed by the 16-bit Column Address and 8-bit dummy clocks or a 24-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first.
The instruction is completed by driving CS# high.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

[Figure 11-2] Read Data (03h) Timing

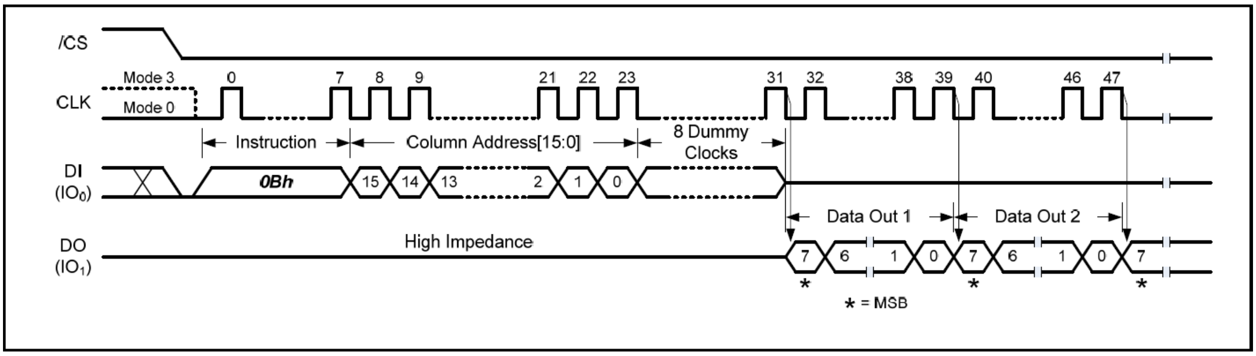


11.3 Fast Read (0Bh)

The Fast Read instruction allows one or more data bytes to be sequentially read from the Data Buffer after executing the Read Page Data instruction. The Fast Read instruction is initiated by driving the CS# pin low and then shifting the instruction code “0Bh” followed by the 16-bit Column Address and 8-bit dummy clocks or a 32-bit dummy clocks into the DI pin. After the address is received, the data byte of the addressed Data Buffer location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first.
The instruction is completed by driving CS# high.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

[Figure 11-3] Fast Read (0Bh) Timing

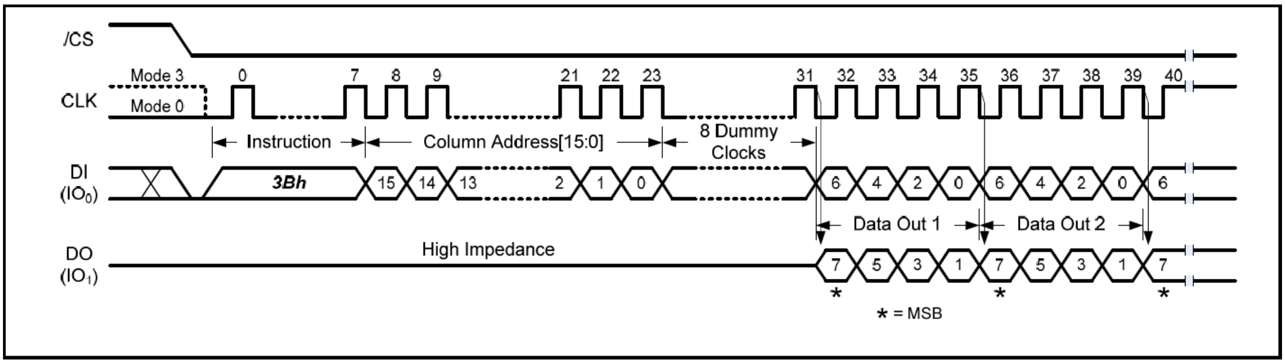


11.4 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard Fast Read (0Bh) instruction except that data is output on two pins; IO0 and IO1. This allows data to be transferred at twice the rate of standard SPI devices.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

[Figure 11-4] Fast Read Dual Output (3B) Timing



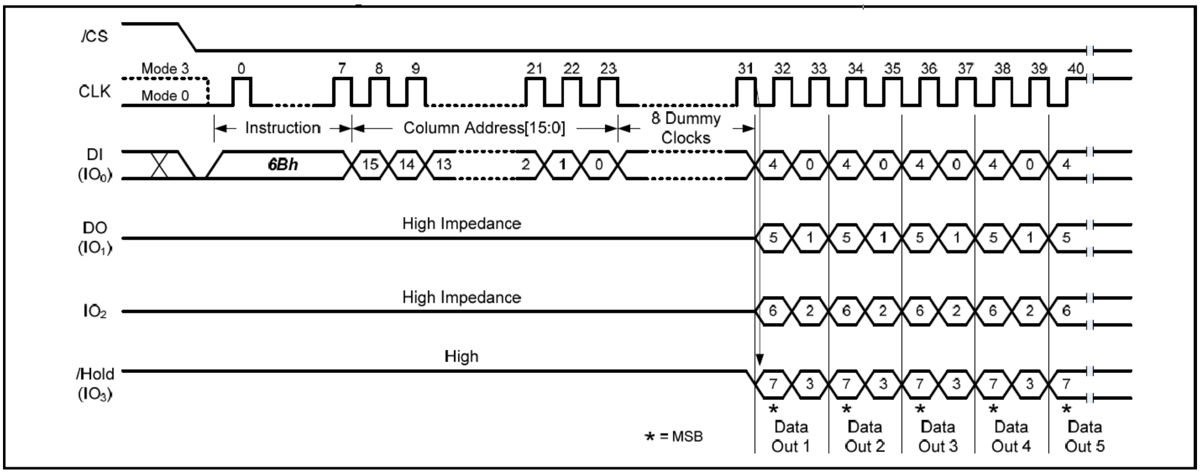
11.5 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the Fast Read Dual Output (3Bh) instruction except that data is output on four pins, IO0, IO1, IO2, and IO3. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

[Figure 11-5] Fast Read Quad Output (6Bh) Timing

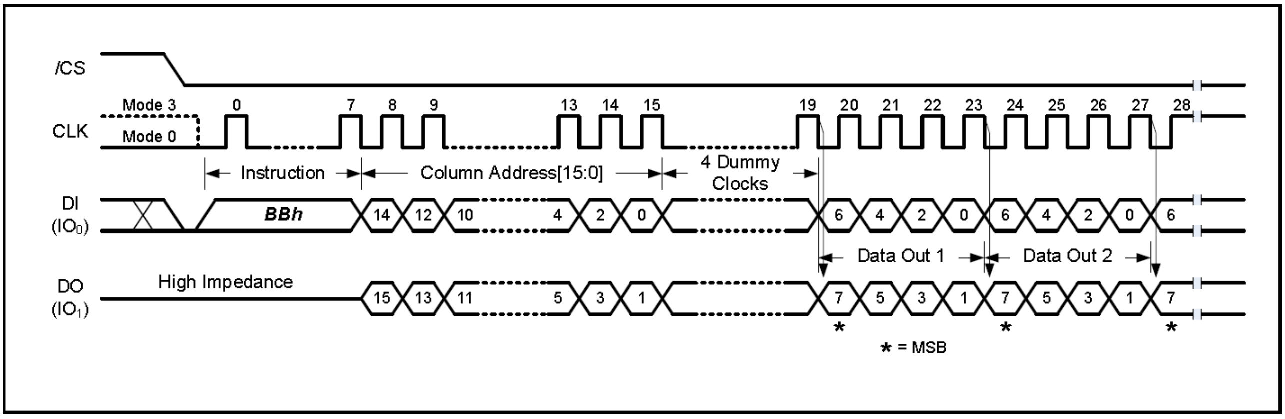


11.6 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Column Address or the dummy clocks two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

[Figure 11-6] Fast Read Dual I/O (BBh) Timing



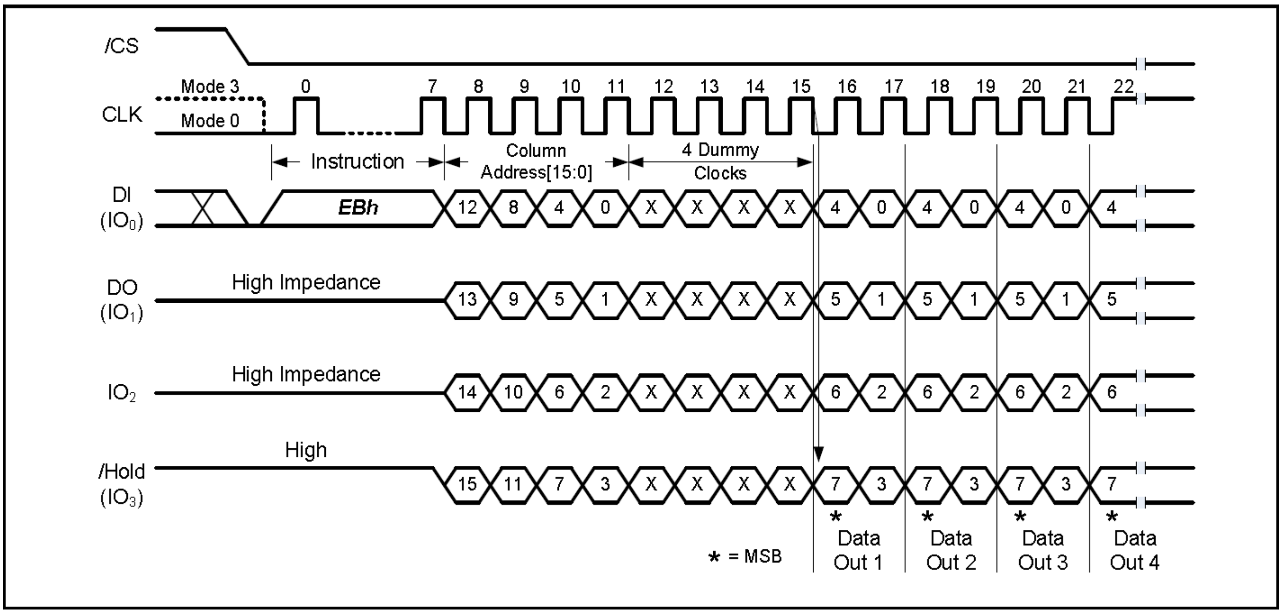
11.7 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI.

The data output sequence will start from the Data Buffer location specified by the 16-bit Column Address and continue to the end of the Data Buffer. Once the last byte of data is output, the output pin will become Hi-Z state.

When WP-E bit in the Status Register is set to a 1, this instruction is disabled.

[Figure 11-7] Fast Read Quad I/O (EBh) Timing



11.8 Accessing Unique ID / Parameter / OTP Pages (OTP-E=1)

In addition to the main memory array, the GSS01GSAX1-W8NMI0 serial product is also equipped with one Unique ID Page, one Parameter Page, and ten OTP Pages.

[Table 11-8] OTP Area Address

Page Address	Page Name	Descriptions	Data Length
00h	Unique ID Page	Factory programmed, Read Only	32-Byte x 16
01h	Parameter Page	Factory programmed, Read Only	256-Byte x 3
02h	OTP Page [0]	Program Only, OTP lockable	2,112-Byte
…	OTP Pages [1:8]	Program Only, OTP lockable	2,112-Byte
0Bh	OTP Page [9]	Program Only, OTP lockable	2,112-Byte

To access these additional data pages, the OTP-E bit in Status Register-2 must be set to “1” first. Then, Read operations can be performed on Unique ID and Parameter Pages, Read and Program operations can be performed on the OTP pages if it’s not already locked. To return to the main memory array operation, OTP-E bit needs to be to set to 0.

Read Operations

A “Page Data Read” command must be issued followed by a specific page address shown in the table above to load the page data into the main Data Buffer. After the device finishes the data loading (BUSY=0), all Read commands may be used to read the Data Buffer starting from any specified Column Address. Please note all Read commands must now follow the “Buffer Read Mode” command structure (CA[15:0], number of dummy clocks) regardless the previous BUF bit setting. ECC can also be enabled for the OTP page read operations to ensure the data integrity.

Program and OTP Lock Operations

OTP pages provide the additional space (2K-Byte x 10) to store important data or security information that can be locked to prevent further modification in the field. These OTP pages are in an erased state set in the factory, and can only be programmed (change data from "1" to "0") until being locked by OTP-L bit in the Configuration/Status Register-2. OTP-E must be first set to "1" to enable the access to these OTP pages, then the program data must be loaded into the main Data Buffer using any "Program Data Load" commands. The "Program Execute" command followed by a specific OTP Page Address is used to initiate the data transfer from the Data Buffer to the OTP page. When ECC is enabled, ECC calculation will be performed during "Program Execute", and the ECC information will be stored into the 64-Byte spare area.

Once the OTP pages are correctly programmed, OTP-L bit can be used to permanently lock these pages so that no further modification is possible. While still in the "OTP Access Mode" (OTP-E=1), user needs to set OTP-L bit in the Configuration/Status Register-2 to "1", and issue a "Program Execute" command(Page address is "don't care"). After the device finishes the OTP lock setting (BUSY=0), the user can set OTP-E to "0" to return to the main memory array operation.

11.9 Parameter Page Data Definitions

The Parameter Page contains 3 identical copies of the 256-Byte Parameter Data. The table below lists all the key data byte locations. All other unspecified byte locations have 00h data as default.

[Table 11-9] OTP Area Address

Byte Number	Descriptions	Values
0~3	Parameter page signature	4Fh, 4Eh, 46h, 49h
4~5	Revision number	00h, 00h
6~7	Feature supported	00h, 00h
8~9	Optional command supported	02h, 00h
10~31	Reserved	All 00h
32~43	Device manufacturer (United Memory)	55h, 6Eh, 69h, 74h, 65h, 64h, 4Dh,65h,6Dh,6Fh,72h,79h
44~63	1 Gb Device model: (GSS01GSAX1-W8NMI0)	47h, 53h, 53h, 30h, 31h, 47h, 53h, 41h, 58h, 31h, 2Dh, 57h, 38h,4Eh, 4Dh, 49h, 30h, 20h, 20h, 20h
64	Manufacturer ID	52h
65~66	Date code	00h, 00h
67~79	Reserved	All 00h
80~83	Number of data bytes per page	00h, 08h, 00h, 00h
84~85	Number of spare bytes per page	40h, 00h
86~91	Reserved	All 00h

92~95	Number of pages per block	40h, 00h, 00h, 00h
96~99	Number of blocks per logical unit	1 Gb：00h, 04h, 00h, 00h
100	Number of logical units	01h
101	Number of address bytes	00h
102	Number of bits per cell	01h
103~104	Bad blocks maximum per unit	1 Gb：14h, 00h
105~106	Block endurance	05h, 04h
107	Guaranteed valid blocks at beginning of target	01h
108~109	Block endurance for guaranteed valid blocks	00h, 00h
0110	Number of programs per page	01h
111	Reserved	00h
112	Number of ECC bits	00h
113	Number of plane address bits	00h
114	Multi-plane operation attributes	00h
115~127	Reserved	All 00h
128	I/O pin capacitance, maximum	08h
129~132	Reserved	All 00h
133~134	Maximum page program time (us)	20h, 03h(800)
135~136	Maximum block erase time (us)	10h, 27h(10000)
137~138	Maximum page read time (us)	C2h, 01h(450)
139~163	Reserved	All 00h
164~165	Vendor specific revision number	00h, 00h
166~253	Vendor specific	All 00h
254~255	Integrity CRC	80h 14h
256~511	Value of bytes 0~255	
512~767	Value of bytes 0~255	
768+	Reserved	

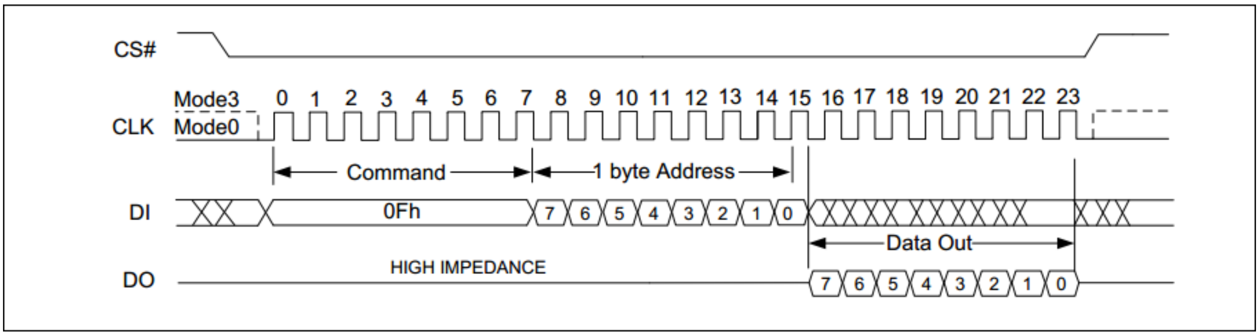
12 Feature Operation

12.1 Read Status Register (0Fh)

The Read Status Register command allow the 8-bit Status Registers to be read. The command is entered by driving CS# low and shifting the command code "0Fh" into the DI pin on the rising edge of CLK followed by an 8-bit Status Register Address. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first.

The Read Status Register command may be used at any time, even while a Program or Erase cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The command is
completed by driving CS# high.

[Figure 12-1] Read Status Register (0Fh) Timing



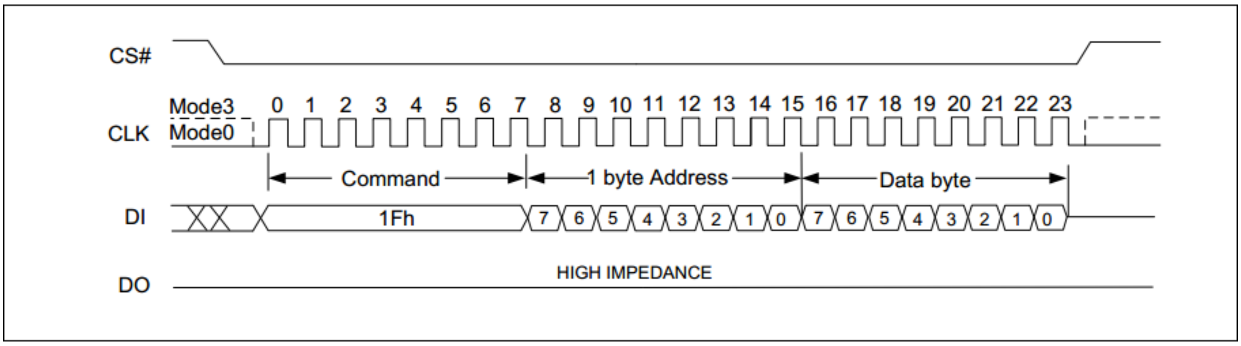
12.2 Write Status Register (1Fh)

The Write Status Register command allows the Status Registers to be written. The writable Status Register bits include: SRP[1:0], TB, BP[3:0] and WP-E bit in Status Register-1; OTP-L, OTP-E and ECC-E bit in Status Register-2. All other Status Register bit locations are read-only and will not be affected by the Write Status Register command.

To write the Status Register bits, the command is entered by driving CS# low, sending the command code "1Fh", followed by an 8-bit Status Register Address, and then writing the status register data byte.

After power up, factory default for BP[3:0], TB, ECC-E bits are 1, while other bits are 0.

[Figure 12-2] Set Features (1Fh) Timing



12.3 Bad Block Management (A1h)

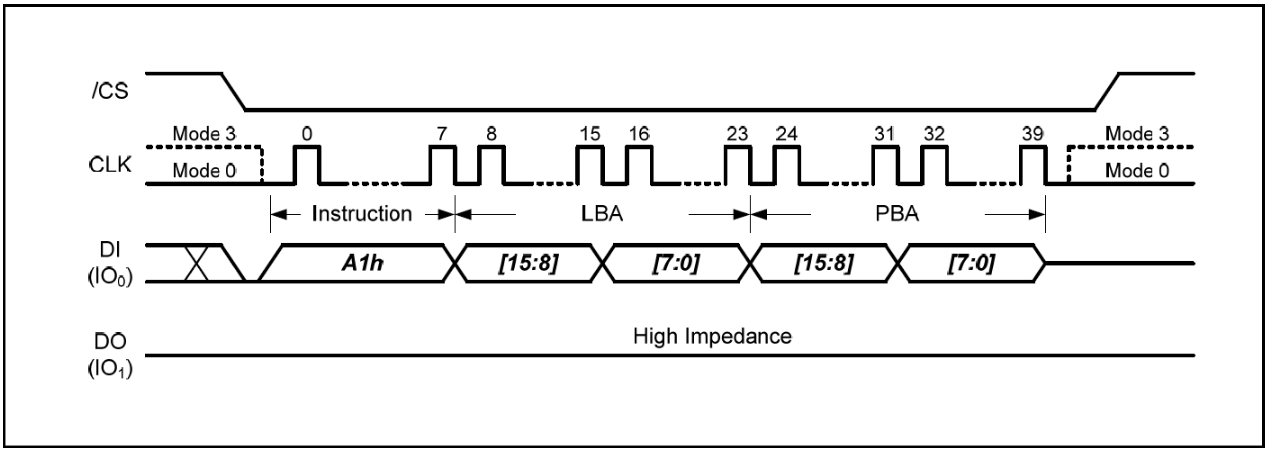
Due to large NAND memory density size and the technology limitation, NAND memory devices are allowed to be shipped to the end customers with certain amount of "Bad Blocks" found in the factory testing. Up to 2% of the memory blocks can be marked as "Bad Blocks" upon shipment, which is a maximum of 20 blocks for GSS01GSAX1-W8NMI0 serial product. In order to identify these bad blocks, it is recommended to scan the entire memory array for bad block markers set in the factory. A "Bad Block Marker" is a non-FFh data byte stored at Byte 0 of Page 0 for each bad block. An additional marker is also stored in the first byte of the 64-Byte spare area.

GSS01GSAX1-W8NMI0 serial product offers a convenient method to manage the bad blocks typically found in NAND flash memory after extensive use. The "Bad Block Management" command is initiated by shifting the instruction code "A1h" into the DI pin and followed by the 16-bit "Logical Block Address" and 16-bit "Physical Block Address". A Write Enable instruction must be executed before the device will accept the Bad Block Management Instructions (Status Register bit WEL= 1). The logical block address is the address for the "bad" block that will be replaced by the "good" block indicated by the physical block address.

Once a Bad Block Management command is successfully executed, the specified LBA-PBA link will be added to the internal Look Up Table (LUT). Up to 20 links can be established in the non-volatile LUT. If all 20 links have been written, the LUT-F bit in the Status Register will become a 1, and no more LBA-PBA links can be established. Therefore, prior to issuing the Bad Block Management command, the LUT-F bit value can be checked or a "Read BBM Look Up Table" command can be issued to confirm if spare links are still available in the LUT.

Registering the same address in multiple PBAs is prohibited. It may cause unexpected behavior.

[Figure 12-3] Bad Block Management (A1h) Timing



12.4 Read BBM Look Up Table (A5h)

The internal Look Up Table (LUT) consists of 20 Logical-Physical memory block links (from LBA0/PBA0 to LBA19/PBA19). The "Read BBM Look Up Table" command can be used to check the existing address links stored inside the LUT.

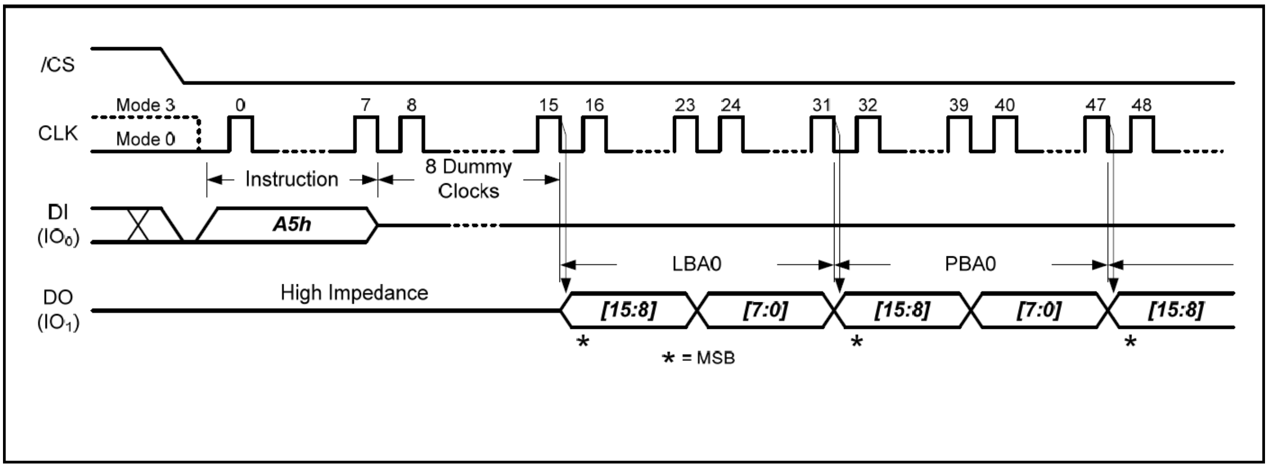
The "Read BBM Look Up Table" command is initiated by shifting the instruction code "A5h" into the DI pin and followed by 8-bit dummy clocks, at the falling edge of the 16th clocks, the device will start to output the 16-bit "Logical Block Address" and the 16-bit "Physical Block Address". All block address links will be output sequentially starting from the first link (LBA0 & PBA0) in the LUT. If there are available links that are unused, the output will contain all "00h" data.

The MSB bits LBA[15:14] of each link are used to indicate the status of the link.

[Table 12-4] Features Settings

LBA[15] (Enable)	LBA[14] (Invalid)	Descriptions
0	0	This link is available to use.
1	0	This link is enabled and it is a valid link.
1	1	This link was enabled, but it is not valid any more.
0	1	Not applicable.

[Figure 12-4] Bad Block Management (A1h) Timing



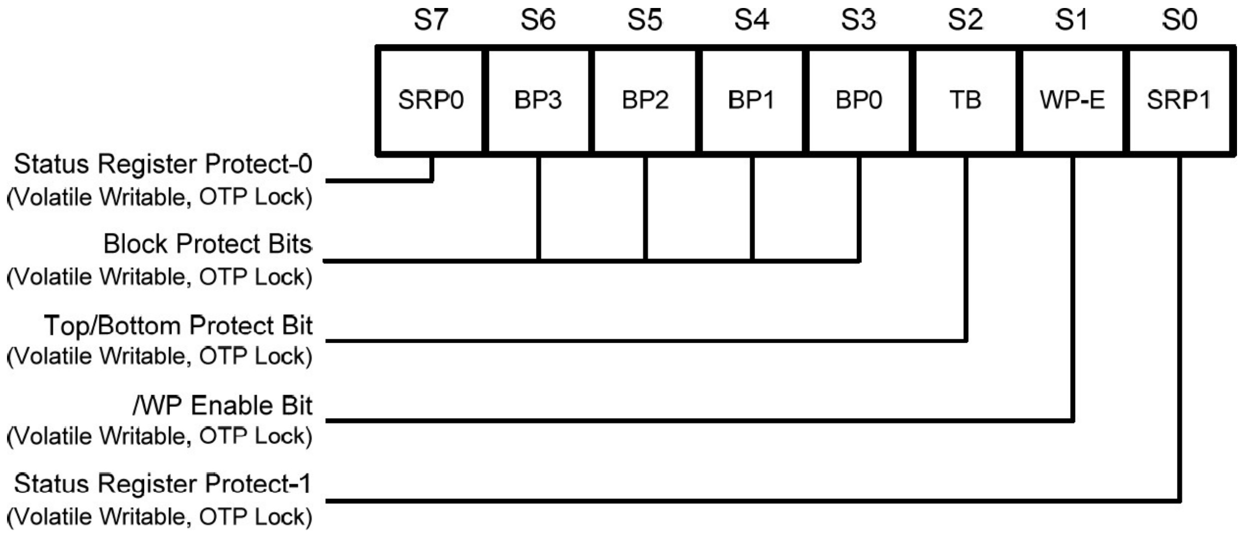
13 Protection, Configuration and Status Registers

Three Status Registers are provided for GSS01GSAX1-W8NMI0 serial product: Protection Register (SR-1), Configuration Register (SR-2) & Status Register (SR-3). Each register is accessed by Read Status Register and Write Status Register commands combined with 1-Byte Register Address respectively.

The Read Status Register instruction (0Fh) can be used to provide status on the availability of the flash memory array, whether the device is write enabled or disabled, the state of write protection, Read modes, Protection Register/OTP area lock status, Erase/Program results, ECC usage/status. The Write Status Register instruction can be used to configure the device write protection features, Software/Hardware write protection, Read modes, enable/disable ECC, Protection Register/OTP area lock. Write access to the Status Register is controlled by the state of the non-volatile Status Register Protect bits (SRP0, SRP1), the Write Enable instruction, and when WP-E is set to 1, the /WP pin.

13.1 Protection Register / Status Register-1

[Figure 13-1] Protection Register / Status Register-1 (Address A0h)



13.1.1 Block Protec Bits

The Block Protect bits (BP3, BP2, BP1, BP0 & TB) are volatile read/write bits in the status register-1 (S6, S5, S4, S3 & S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction. All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The default values for the Block Protection bits are 1 after power up to protect the entire array.

13.1.2 Write Protection Enable Bit (WP-E)

The Write Protection Enable bit (WP-E) is a volatile read/write bits in the status register-1 (S1). The WP-E bit, in conjunction with SRP1 & SRP0, controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection, /WP pin functionality, and Quad SPI operation enable/disable. When WP-E = 0 (default value), the device is in Software Protection mode, /WP & /HOLD pins are multiplexed as IO pins, and Quad program/read functions are enabled all the time. When WP-E is set to 1, the device is in Hardware Protection mode, all Quad functions are disabled

13.1.3 Status Register Protec Bits (SPR1, SPR0)

The Status Register Protect bits (SRP1 and SRP0) are volatile read/write bits in the status register (S0 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

[Table 13-1] Software Protection

Software Protection (Driven by Controller, Quad Program/Read is enabled)				
SPR1	**SPR0**	**WP-E**	**/WP / IO2**	**Descriptions**
0	0	0	X	No /WP functionality /WP pin will always function as IO2
0	1	0	0	SR-1 cannot be changed (/WP = 0 during Write Status) /WP pin will function as IO2 for Quad operations
0	1	0	1	SR-1 can be changed (/WP = 1 during Write Status) /WP pin will function as IO2 for Quad operations
1	0	0	X	Power Lock Down(1) SR-1 /WP pin will always function as IO2

[Table 13-2] Hardware Protection

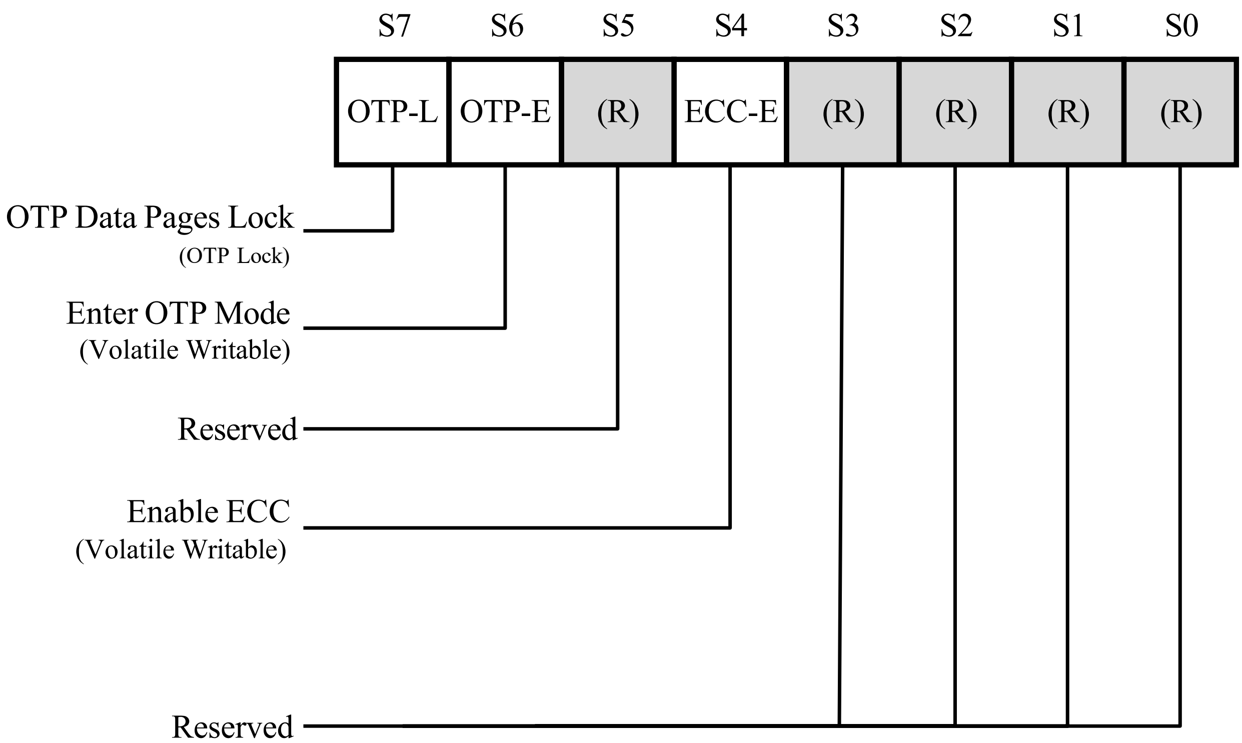
Hardware Protection (System Circuit / PCB layout, Quad Program/Read is disabled)				
SPR1	**SPR0**	**WP-E**	**/WP Only**	**Descriptions**
0	X	1	VCC	SR-1 can be changed
1	0	1	VCC	Power Lock=Down(1) SR-1
X	X	1	GND	All "Write / Program / Erase" command are blocked Entire device (SRs, Array, OTP area) is read-only

Note:

1. When SRP1, SRP0 = (1, 0), a power-down, power-up cycle will change SRP1, SRP0 to (0, 0) state.

13.2 Configuration Register / Status Register-2

[Figure 13-2] Configuration Register / Status Register-2 (Address B0h)



13.2.1 One Time Program Lock Bit (OTP-L) – *OTP Lockable*

In addition to the main memory array, GSS01GSAX1-W8NMI0 serial product also provides an OTP area for the system to store criticaldata that cannot be changed once it’s locked. The OTP area consists of 10 pages of 2,112-Byte each. The default data in the OTP area are FFh. Only Program command can be issued to the OTP area to change the data from “1” to “0”, and data is not reversible (“0” to “1”) by the Erase command. Once the correct data is programmed in and verified, the system developer can set OTP-L bit to 1, so that the entire OTP area will be locked to prevent further alteration to the data.

13.2.2 Enter OTP Access Mode Bit (OTP-E) – *Volatile Writable*

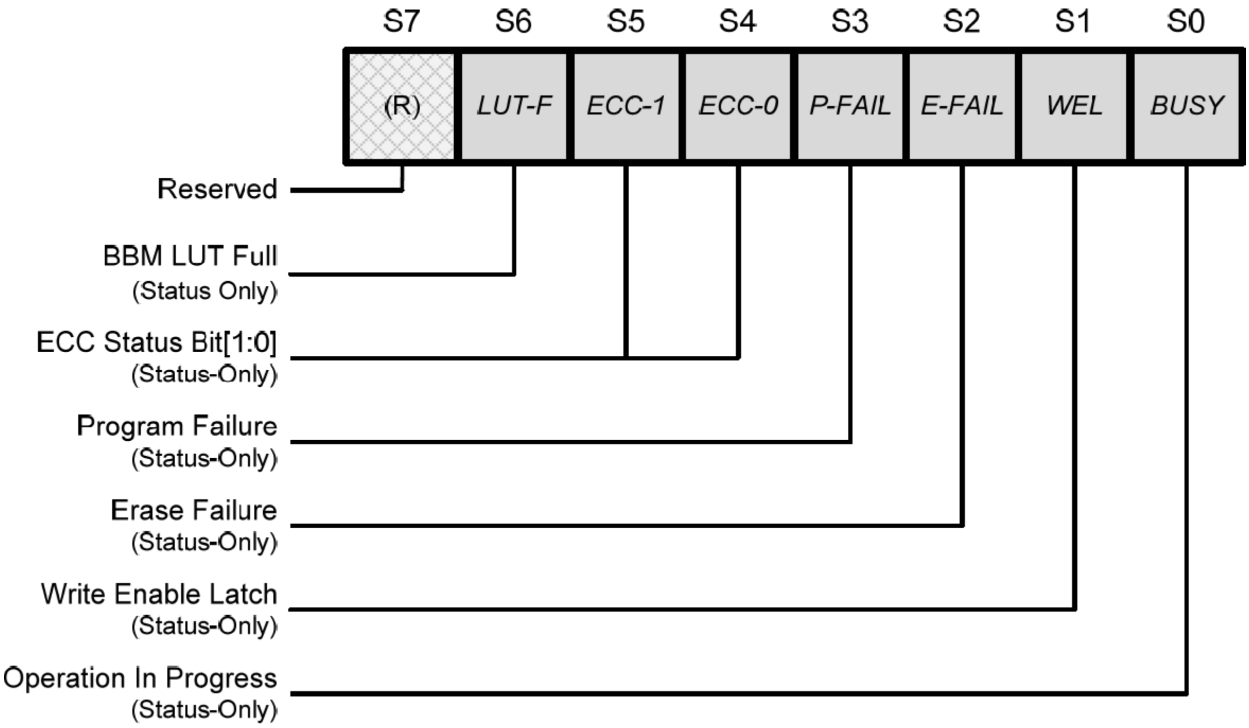
This device offers a protected, one-time programmable NAND Flash memory area. Ten full pages (10 x 2112 bytes per page) per die are available, and the entire range is guaranteed. Customers can choose how to use the OTP area, such as programming serial numbers or other data for permanent storage. The OTP area can't be erased. When ECC is enabled, data written in the OTP area is ECC protected. Besides some additional configuration bits are described in this section.

13.2.3 ECC Enable Bit (ECC-E) – *Volatile Writable*

GSS01GSAX1-W8NMI0 serial product has a built-in ECC algorithm that can be used to preserve the data integrity. Internal ECC calculation is done during page programming, and the result is stored in the extra 64-Byte area for each page. During the data read operation, ECC engine will verify the data values according to the previously stored ECC information and to make necessary corrections if needed. The verification and correction status is indicated by the ECC Status Bits. ECC function is enabled by default when power on (ECC-E=1), and it will not be reset to 0 by the Device Reset command.

13.3 Status Register-3 (Status Only)

[Figure 13-3] Status Register-3 (Address C0h)



13.3.1 Look-Up Table Full (LUT-F) – *Status Only*

To facilitate the NAND flash memory bad block management, the GSS01GSAX1-W8NMI0 serial product is equipped with an internal Bad Block Management Look-Up-Table (BBM LUT). Up to 20 bad memory blocks may be replaced by a good memory block respectively. The addresses of the blocks are stored in the internal Look-Up Table as

Logical Block Address (LBA, the bad block) & Physical Block Address (PBA, the good block). The LUT-F bit indicates whether the 20 memory block links have been fully utilized or not. The default value of LUT-F is 0, once all 20 links are used, LUT-F will become 1, and no more memory block links may be established.

13.3.2 Cumulative ECC Status (ECC-1, ECC-0) – *Status Only*

ECC function is used in NAND flash memory to correct limited memory errors during read operations. The ECC Status Bits (ECC-1, ECC-0) should be checked after the completion of a Read operation to verify the data integrity. The ECC Status bits values are don’t care if ECC-E=0. These bits will be cleared to 0 after a power cycle or a RESET command.

[Table 13-3] ECC Status

ECC Status		Descriptions
ECC-1	ECC-0	
0	0	Entire data output is successful, with 0-6bit/512bytes ECC corrections in a single/multiple page.
0	1	Entire data output is successful, with 7-8 bit/512bytes ECC corrections in a single/multiple page.
1	0	Entire data output contains more than 8 bits errors only in a single page which cannot be repaired by ECC.

13.3.3 Program/Erase Failure (P-FAIL, E-FAIL) – *Status Only*

The Program/Erase Failure Bits are used to indicate whether the internally-controlled Program/Erase operation was executed successfully or not. These bits will also be set respectively when the Program or Erase command is issued to a locked or protected memory array or OTP area. Both bits will be cleared at the beginning of the Program Execute or Block Erase instructions as well as the device RESET instruction.

13.3.4 Write Enable Latch (WEL) – *Status Only*

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to 1 after executing a Write Enable Instruction. The WEL status bit is cleared to 0 when the device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Program Execute, Block Erase, Page Data Read, Program Execute and Bad Block Management for OTP pages.

13.3.5 Erase/Program In Progress (Busy) – *Status Only*

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is powering up or executing a Page Data Read, Bad Block Management, Program Execute, Block Erase, Program Execute for OTP area. During this time the device will ignore
further instructions except for the Read Status Register and Read JEDEC ID instructions. When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

13.3.6 Reserved Bits – *Non Functional*

There are a few reserved Status Register bits that may be read out as a “0” or “1”. It is recommended to ignore the values of those bits. During a “Write Status Register” instruction, the Reserved Bits can be written as “0”, but there will not be any effects.

13.4 Status Register Memory Protection

[Table 13-4] Memory Protection 1 Gb

STATUS REGISTER (1)					(1G-Bit / 128M-Byte) Memory Protection(2)			
TB	BP3	BP2	BP1	BP0	Protected Block(s)	Protected Page Address PA[15:0]	Protected Density	Protected Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	1022 & 1023	FF80h～FFFFh	256KB	Upper 1/512
0	0	0	1	0	1020 thru1023	FF00h～FFFFh	512KB	Upper 1/256
0	0	0	1	1	1016 thru1023	FE00h～FFFFh	1MB	Upper 1/128
0	0	1	0	0	1008 thru1023	FC00h～FFFFh	2MB	Upper 1/64
0	0	1	0	1	992 thru1023	F800h～FFFFh	4MB	Upper 1/32
0	0	1	1	0	960 thru1023	F000h～FFFFh	8MB	Upper 1/16
0	0	1	1	1	896 thru1023	E000h～FFFFh	16MB	Upper 1/8
0	1	0	0	0	768 thru1023	C000h～FFFFh	32MB	Upper 1/4
0	1	0	0	1	512 thru1023	8000h～FFFFh	64MB	Upper 1/2
1	0	0	0	1	0 & 1	0000h～007Fh	256KB	Lower 1/512
1	0	0	1	0	0 thru 3	0000h～00FFh	512KB	Lower 1/256
1	0	0	1	1	0 thru 7	0000h～01FFh	1MB	Lower 1/128
1	0	1	0	0	0 thru 15	0000h～03FFh	2MB	Lower 1/64
1	0	1	0	1	0 thru 31	0000h～07FFh	4MB	Lower 1/32
1	0	1	1	0	0 thru 63	0000h～0FFFh	8MB	Lower 1/16
1	0	1	1	1	0 thru 127	0000h～1FFFh	16MB	Lower 1/8
1	1	0	0	0	0 thru 255	0000h～3FFFh	32MB	Lower 1/4
1	1	0	0	1	0 thru 511	0000h～7FFFh	64MB	Lower 1/2
X	1	0	1	X	0 thru 1023	0000h～FFFFh	128MB	ALL
X	1	1	X	X	0 thru 1023	0000h～FFFFh	128MB	ALL

Notes:

1) X = don’t care
2) If any Erase or Program command specifies a memory region that contains protected data portion, this command will be ignored.

14 ECC Protection

The device offers an 8-bit data corruption protection by offering internal ECC to obtain the data integrity. The internal ECC can be enabled or disabled by setting the ECC_EN bit in the configuration register. ECC is enabled after device power-up by default. The READ and PROGRAM commands operate with internal ECC by default. Reset will not change the existing configuration.
To enable/disable ECC after power on, perform the following command sequence:

- Issue the SET FEATURES command (1Fh)
- Issue configuration register address (B0h)
- Then: To enable ECC, set bit 4 (ECC enable) to 1; To disable ECC, clear bit 4 (ECC enable) to 0

During a PROGRAM operation, the device calculates an expected ECC code on the ECC protected bytes in the cache register, before the page is written to the NAND Flash array. The ECC code is stored in the spare area of the page.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the expected ECC code value read from the array. If a 1–8-bit error is detected, the error is corrected in the cache register. Only corrected data is output on the I/O bus. The ECC status register bit indicates whether or not the error correction is successful. The table below describes the ECC protection scheme used throughout a page.

With internal ECC, users must accommodate the following (details provided in table below):
- Spare area definitions provided in the ECC Protection table below
- ECC can protect according main and spare areas. WRITEs to the ECC area are prohibited

Power on Read with internal ECC:
The device will automatically read first page of first block to cache after power on, then host can directly read data from cache for easy boot. Also the data is promised correctly by internal ECC.

[Table 14-1] ECC Protection and Spare Area

Min Byte Address	Max Byte Address	ECC protected	Area	Description
000h	1FFh	YES	Sector 0	User data 0
200h	3FFh	YES	Sector 1	User data 1
400h	5FFh	YES	Sector 2	User data 2
600h	7FFh	YES	Sector 3	User data 3
800h	83Fh	YES	Spare Area	User Meta Area
840h	84Fh	YES	Spare Area	Sector 0 ECC parity data
850h	85Fh	YES	Spare Area	Sector 1 ECC parity data
860h	86Fh	YES	Spare Area	Sector 2 ECC parity data
870h	87Fh	YES	Spare Area	Sector 3 ECC parity data

Notes:
Byte 2048 of page 0 for each block is “Bad Block Marker”.

15 Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in the table below. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more bad bits than can be corrected by the minimum required ECC. Additional bad blocks may develop with use. However, the total number of available blocks will not fall below NVB during the endurance life of the product.

Although NAND Flash memory devices may contain bad blocks, they can be used reliably in systems that provide bad-block management and error-correction algorithms. This ensures data integrity.

Internal circuitry isolates each block from other blocks, so the presence of a bad block does not affect the operation of the rest of the NAND Flash array.

NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark into every location in the first page of each invalid block. It may not be possible to program every location in an invalid block with the bad-block mark. However, the first spare area location in each bad block is guaranteed to contain the bad-block mark. This method is compliant with ONFI factory defect mapping requirements. See the following table for the bad-block mark.

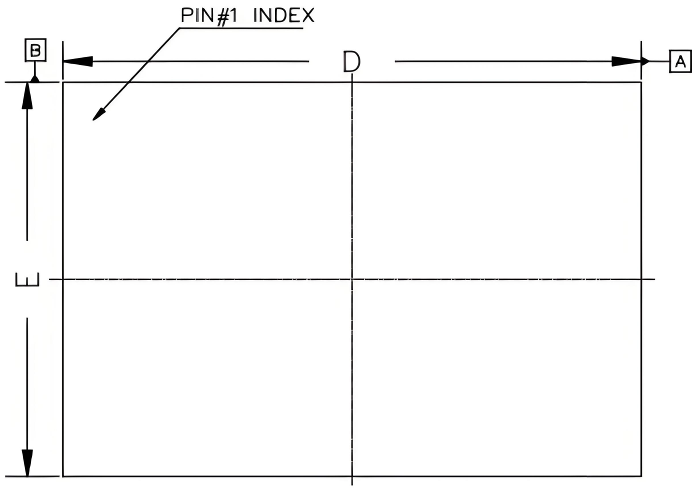
System software should initially check the first spare area location for non-FFh data on the first page of each block prior to performing any program or erase operations on the NAND Flash device. A bad-block table can then be created, enabling system software to map around these areas. Factory testing is performed under worst-case conditions. Because invalid blocks may be marginal, it may not be possible to recover the bad-block marking if the block is erased.

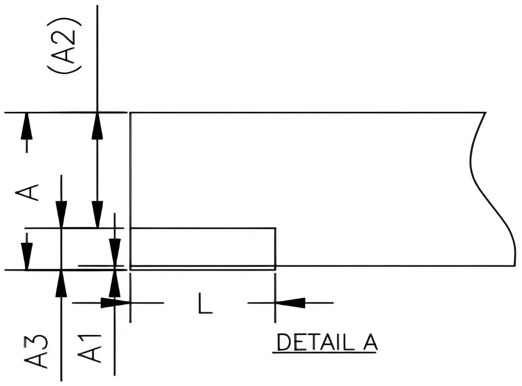
[Table 15-1] Error Management Details

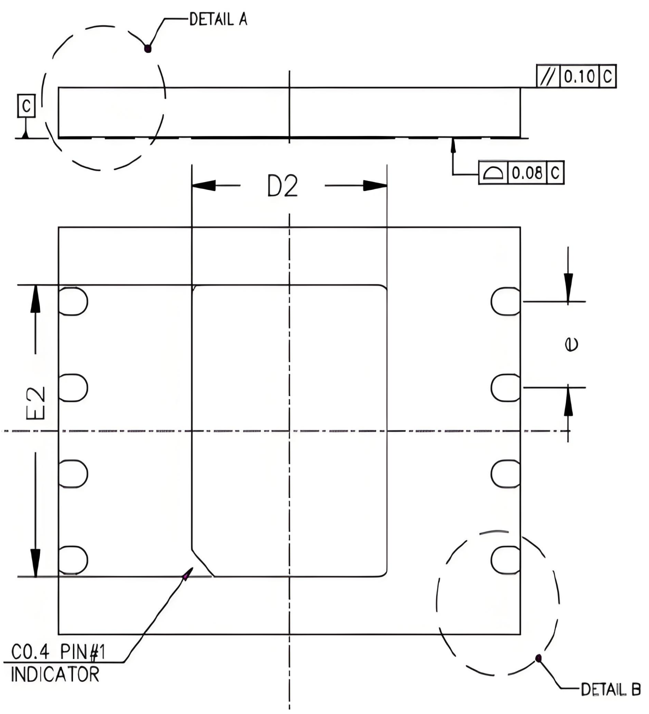
Description	Requirement
	1Gb
Minimum number of valid blocks (NVB)	1004
Total available blocks	1024
First Spare area location	Byte 2048
Bad block mark	Non FFh
Minimum required ECC	8-bit ECC per sector (512) bytes of data

16 Package Dimensions

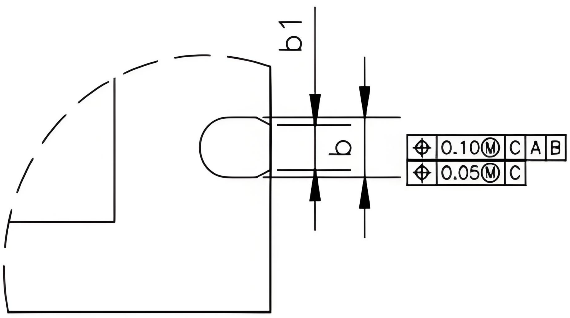
[Finger 16-1] 8-pin WSON 8mm x 6mm x 0.8mm







SYMBOL	DIMENSION (MM)		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3	-	0.20	-
b	0.35	0.40	0.45
b1		0.30 Ref.	
D	7.90	8.00	8.10
D2	3.30	3.40	3.50
E	5.90	6.00	6.10
E2	4.20	4.30	4.40
e		1.27 BSC	
L	0.40	0.50	0.60



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